QUANTUM

SERVICE
MANUAL

Q2000
8″ Media Fixed Disk Drive

SERIES 2000
DISK DRIVES

Maintenance Manual
P R E L I M I N A R Y

81-40238 Rev A

September 1981

QUANTUM, INC.

PREFACE

This is a PRELIMINARY manual. It may not contain certain items of information not available at the time of printing. These omissions are noted, where possible, in the manual.

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Publication No. 81-40238, Rev. A - First Edition (Preliminary)

WARRANTY

Quantum Series 2000 disk drives are warranted against defects in materials and workmanship for 1 year from the date of shipment. Any questions regarding the warranty should be directed to your Quantum Sales Representative. All requests for repair should be directed to the Quantum Service Center in your area. This will assure you of the fastest possible service.

UL/CSA

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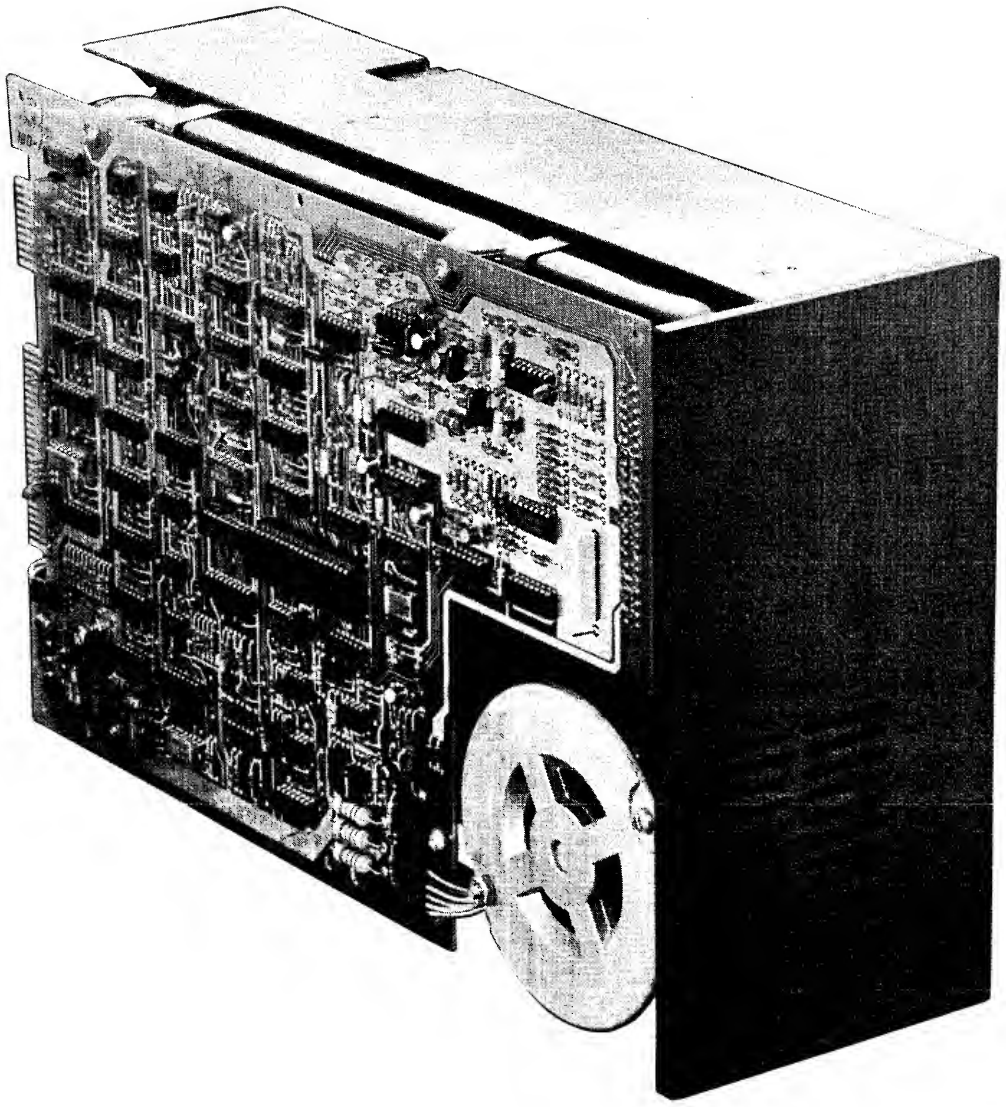

FIGURE 1-1
SERIES 2000 DRIVE

SECTION 1

GENERAL DESCRIPTION & SPECIFICATIONS

1.1 GENERAL DESCRIPTION

Quantum's Series 2000 Disk Drives are random access storage devices using one to four non-removable 8" rigid disk platters as storage media. Each disk platter has two surfaces each employing one movable head to access the 512 data tracks. Using a rotary positioner with its inherent simplicity of mechanical construction and electronic control both low cost and high reliability are achieved. The Series 2000 is available in four models: the Q2010 having an unformatted 10.66 Mb capacity on one disk platter and two heads, the Q2020, having an unformatted 21.33 Mb capacity on two disk platters and four heads, the Q2030 having an unformated 32.00 Mb capacity on three disk platters and six heads, and the Q2040 having and unformatted 42.66 Mb capacity on four disk platters and eight heads.

1.2 SPECIFICATIONS

The Series 2000 disks drives have the following key features:

- Storage capacity of 10, 20, 30 or 40 megabytes
- Winchester design reliability
- Same physical size and mounting as 8" floppy drives
- Actuator and spindle locks to hold heads on a landing zone outside the data area during shipping
- Proprietary, high resolution, quiet, rotary head position actuator
- 4.34M bits/second transfer rate
- Microprocessor controlled temperature compensation servo
- Uses the same DC voltages as 8" floppy drives

1.2.1 PHYSICAL SPECIFICATIONS

Environmental Limits

Ambient temperature -
Storage: 50°F to 150°F (10°C to 65.5°C)
Shipping: -40°F to 144°F (-40°C to 62°C)
Operating: 50° to 115°F (10°C to 46°C)

Ambient Relative Humidity -
Storage: 1% to 95% without condensation
Shipping: 1% to 95% without condensation
Operating: 8% to 80% without condensation

Maximum wet bulb = 78° non-condensing

Altitude -
Storage: -1000 Ft. to 40,000 Ft.
Shipping: -1000 Ft. to 40,000 Ft.
Operating (max.): 10,000 Ft. (3048 Meters)

AC Power Requirements

50 or 60Hz ± 0.5Hz
100/115VAC Installations = 90-127 at 1.0A Typical, 4.0A max
200/230VAC Installations = 180-253V at 0.5A Typical, 2.0a max

DC Voltage Requirements

+24VDC±10% 1.25A Typical, 1.5A maximum
+5VDC±5% 1.0A Typical, 1.5A maximum
-5VDC±5% (-7 to -16 VDC optional) 0.20A Typical, .25A Maximum

Mechancial Dimensions

Height = 4.50 in. (114.3mm)
Width = 8.55 in. (217.2mm)
Depth = 14.25 in. (362.0mm)
Weight = 17 lbs. (7.7Kg)

Heat Dissipation

235 BTU/HOUR Typical (70 Watts)

1.2.2 PERFORMANCE SPECIFICATIONS

	Q2010	Q2020	Q2030	Q2040
Capacities				
Unformatted				
Per drive	10.66Mb	21.33Mb	32.00Mb	42.66Mb
Per surface	5.33Mb	5.33Mb	5.33Mb	5.33Mb
Per track	10.40Kb	10.40Kb	10.40Kb	10.40Kb
Formatted (MFM)				
Per drive	8.40Mb	16.80Mb	25.20Mb	33.60Mb
Per surface	4.20Mb	4.20Mb	4.20Mb	4.20Mb
Per track	8.20Kb	8.20Kb	8.20Kb	8.20Kb
Per sector	256 Bytes	256 Bytes	256 Bytes	256 Bytes
Sectors/tk	32	32	32	32
Transfer Rate (MFM)	4.34Mbits/sec	4.34Mbits/sec	4.34Mbits/sec	4.34Mbits/sec
Access Times (All voltages nominal, ambient temperature 25°C)				
TK to TK (max.)	15 ms	15 ms	15 ms	15 ms
Average (max.)	55 ms	60 ms	60 ms	65 ms
Full Stroke (typ.)	100 ms	100 ms	100 ms	105 ms
Avg Latency	10 ms	10 ms	10 ms	10 ms

Access time is the time between the rising edge of seek complete and the falling edge of seek complete. All access time measurements are made at an ambient temperature of 77°F (25°C) with both AC and DC voltages at nominal. The above access times are measured as follows:

1) TK to TK access time is an average of the access times of at least ten (10) single track seeks in each direction.

2) Full stroke access time is an average of the access times of at least ten (10) 511 track seeks in each direction.

3) Average access time is determined by dividing the sum of the access times for all seek lengths in each direction, weighted by the number of possible seeks of each length, by the total number of possible seeks:

Q2000 Average Seek Measurement Algorythm

$$T_A = \sum_{K=1}^{N-1} \frac{(N-K)(0+ + 0-)}{N(N-1)}$$

$$T_A = \sum_{K=1}^{511} \frac{(512-K)(0+ K + 0- K)}{(512)(511)}$$

Where

T_A = Average Access Time

N = Total number of cylinders (starting with 1)

K = Integer which varies to include all possible seek lengths.

0^+K = Inward measured seek time for a K track seek.

0^-K = Outward measured seek time for a K track seek.

2(N-K) = Total Possible Number of seeks of length K

N(N-1) = Total number of possible seeks

Media Quality

All Series 2000 drives are provided with an error map showing media defects. The defective areas are identified by cylinder number, head number, the number of bytes from index and the number of bits in length.

The media is guaranteed to be error free on cylinder 000. Additionally, there will be no more than 12 defects on any surface, and no surface will have more than 4 tracks with multiple defects.

A single defect is defined as an error equal to or less than 16 bits in length. A multiple defect is an error greater than 16 bits in length or a single error in several areas of the same track.

Error Rates

Soft read errors: 1 per 10^{10} bits read
Hard read errors: 1 per 10^{12} bits read
Seek errors: 1 per 10^{6} seeks

1.2.3 FUNCTIONAL SPECIFICATIONS

	Q2010	Q2020	Q2030	Q2040
Rotational speed	3000 RPM	3000 RPM	3000 RPM	3000 RPM
Max Recording Density	6600 bpi	6600 bpi	6600 bpi	6600 bpi
Max Flux Density	6600 fci	6600 fci	6600 fci	6600 fci
Track Density	345 tpi	345 tpi	345 tpi	345 tpi
Cylinders	512	512	512	512
Tracks	1024	2048	3072	4096
R/W Heads	2	4	6	8
Disks	1	2	3	4
Index	1	1	1	1

1.2.4 RELIABILITY SPECIFICATION

MTBF: 8,000 POH typical usage
PM: not required
MTTR: 30 minutes
Component Life: 5 years

1.2.5 STANDARDS & REGULATIONS

It is intended that the Series 2000 drives will satisfy the following standards and regulations.

UL - Standard 478, Standard for Safety, Electronic Data Processing Units and Systems.

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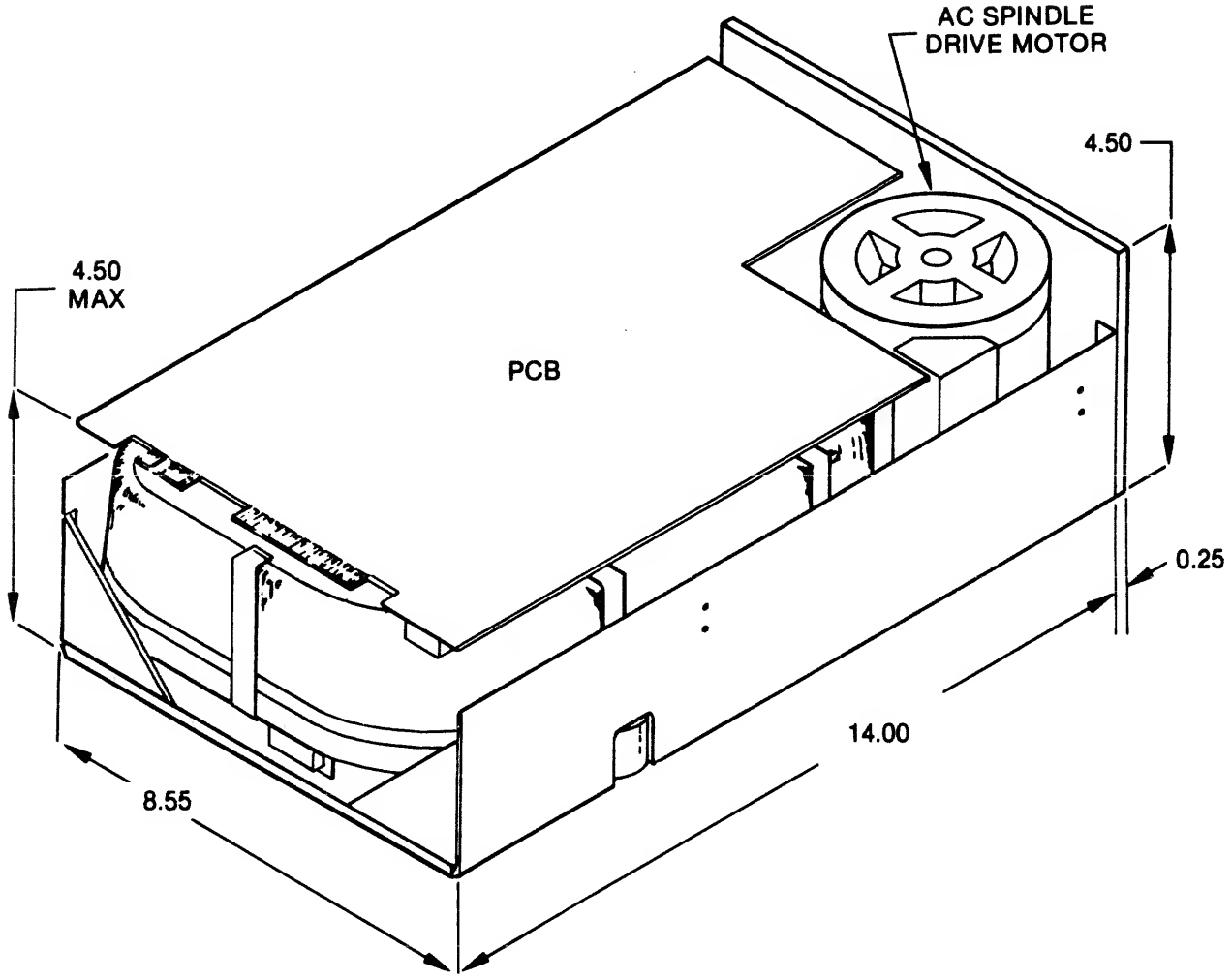
SECTION 2

INSTALLATION AND OPERATION

2.1 INSTALLATION

2.1.1 Space Requirements

The Series 2000 drives are shipped mounted in a cabinet assembly with a face plate installed. Figure 2-1 shows the external dimensions of the drive.



All dimensions in inches

FIGURE 2-1
SERIES 2000 MECHANICAL DIMENSIONS

2.1.2 Unpacking Instructions

1) Open the shipping container
2) Using the handles provided on the inner container, lift the drive and inner container from the shipping container.

   CAUTION: Do Not Lift the drive by the PCB or the face plate.

3) Remove the plastic covering from the Series 2000.
4) Stand the drive on edge to unlock the spindle lock. (See Figure 2-2.)
5) Loosen the 11/32 inch hex nut.
6) Rotate the locking clip away from pulley. DO NOT ROTATE PULLEY.
7) Retighten 11/32 inch hex nut.
8) Unlock the actuator by rotating the actuator lock counter clockwise as far as it will go (approximately 1/2 turn). The embossed arrow will now point to RUN (see Figure 2-3.) DO NOT FORCE.

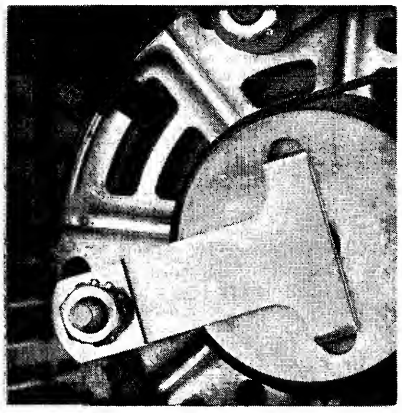


FIGURE 2-2
SPINDLE LOCK

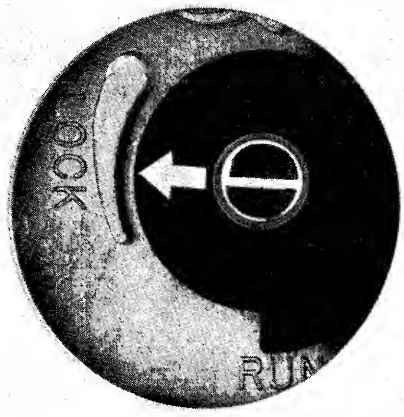


FIGURE 2-3
ACTUATOR LOCK

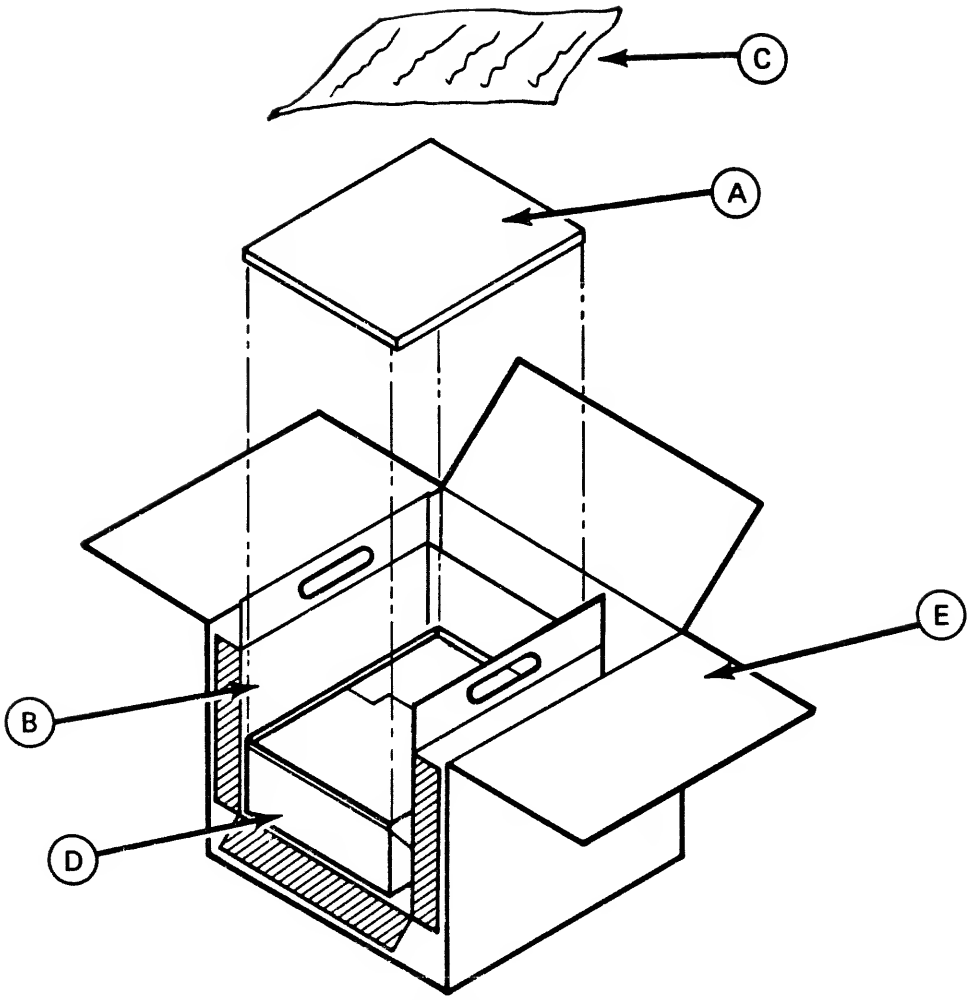


FIGURE 2-4
SERIES 2000 PACKING ASSEMBLY

Figure 2-4 illustrates the packing assembly for the Series 2000 and the following list identifies each item.

ITEM	DESCRIPTION
A	Foam Pad
B	Padded Internal Container
C	Unpacking Instructions
D	Q2000 Disk Drive
E	External Shipping Container

NOTE: After unpacking the Series 2000, store the packing materials for possible future use.

2.1.3 Mounting

The Series 2000 drive may be mounted in any orientation and has mounting holes on three sides for this purpose. Figure 2-5 shows the location of these mounting holes and the location of the access cutouts for the actuator and spindle locks. Free access to these cutouts should be provided in whatever mounting configuration is chosen.

CAUTION

The base casting and plastic enclosure are very close to the cabinet walls. Mounting screw lengths must be chosen so that no more than .125" (3.175 mm) of the screw is available to enter the cabinet mounting holes. See Figure 2-6. This length will allow full use of the mounting hole threads and avoid damaging the enclosure or placing unwanted stress on the base casting.
To avoid stripping the mounting hole threads the maximum torque applied to the mounting screws must not exceed 18 inch/pounds.

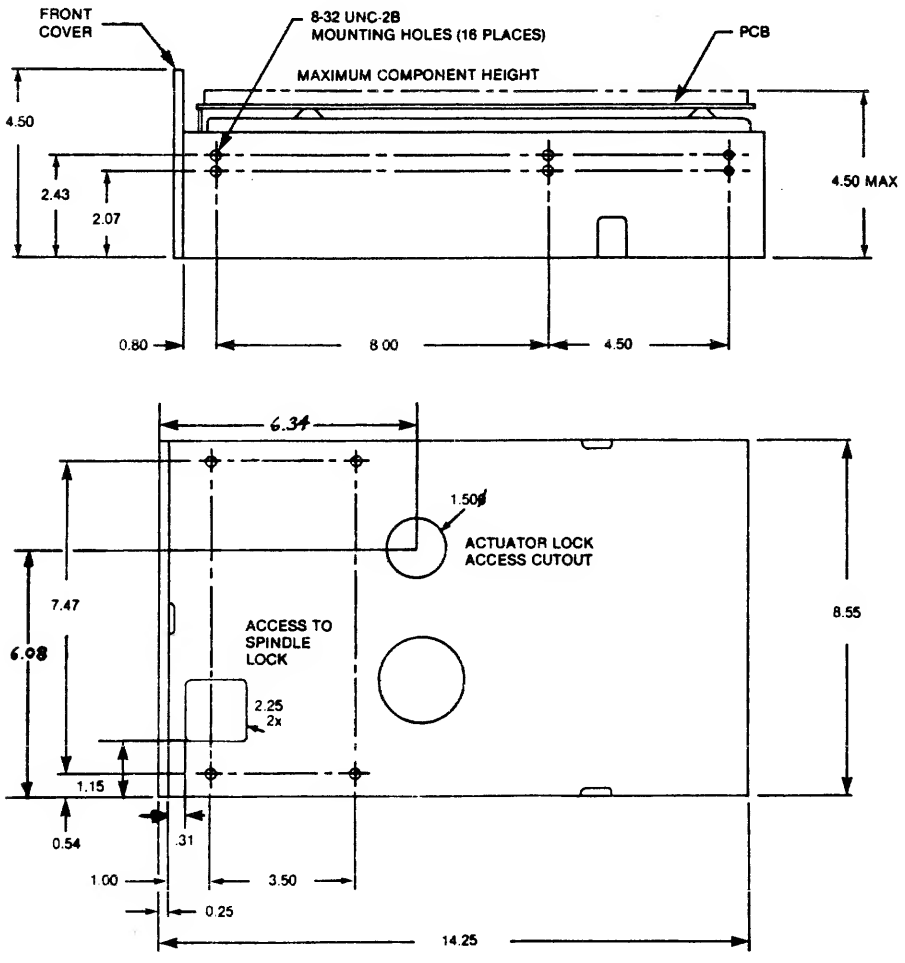


FIGURE 2-5
SERIES 2000 MOUNTING SCREW CLEARANCE

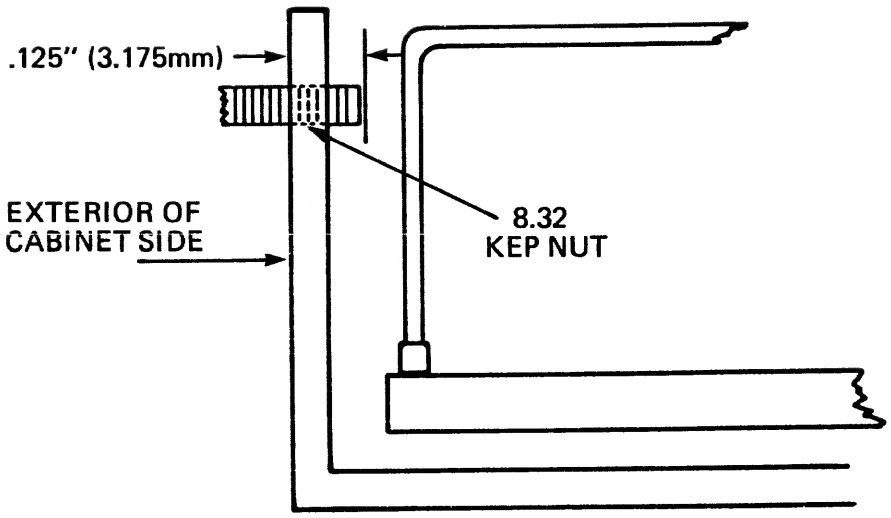


FIGURE 2-6
SERIES 2000 MOUNTING DIMENSIONS

2.1.4 Power Requirements

2.1.4.1 AC Power

The voltage, frequency and current requirements of the AC Power supplied to the Series 2000 drives are given in Table 2-1.

Table 2-1.
AC Power Requirements

	60HZ		50HZ	
CONNECTOR P4 PIN	110V (Standard)	208/230V	100V	220V
1	90-127V	180-253V	90-127V	180-253V
2	FRAME GND	FRAME GND	FRAME GND	FRAME GND
3	90-127 RTN	180-253V	90-127 RTN	180-253V
CURRENT				
MAX RUSH **	4.0 Amps	2.0 Amps	4.0 Amps	2.0 Amps
MAX RUN	1.0 Amps	0.5 Amps	0.7 Amps	0.35 Amps
FREQ TOL	± 0.5HZ		± 0.5HZ	

** In rush duration (at 117 VAC)

1 sec. for Q2010	3 sec. for Q2030
2 sec. for Q2020	4 sec. for Q2040

2.1.4.2 DC Power

The voltages and current requirements of the DC Power supplied to the drive are listed in Table 2-2. No power sequencing either off or on is required by the Series 2000.

Table 2-2.
DC Power Requirements

Voltage			
Nominal	+24V	+5V	-5V (-7 to -16V)
Current			
Typical	1.25A	1.0A	.20A
Maximum	1.5A	1.5A	.25A
Regulation	± 2.4V	±0.25V	±0.25V
Ripple and Noise			
Maximum	1V P-P	50mv P-P	50mv P-P

2.2 INTERCONNECTING CABLE CONNECTORS

2.2.1 AC Power

AC power and frame ground are supplied to the Series 2000 through a 3 pin connector. Refer to Figure 2-7. The pin housing (J4) is mounted in the drive and is AMP P/N 1-480701-0 with pins AMP P/N 350687-1 and 350654-1 (gnd pin). The recommended mating connector (P4) is AMP socket P/N 1-480700-0 with AMP pins P/N 350536-1.

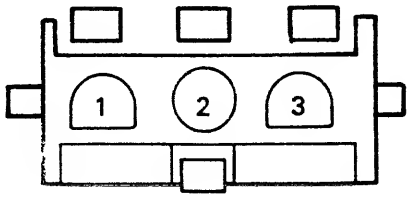


FIGURE 2-7
J4 CONNECTOR

The disk drive is shipped with DC ground (base casting) and AC ground (drive motor) connected together with a ground strap located on the drive motor and base casting. AC and DC grounds may be separated by removing the ground wire connected between the AC motor and the base casting.

2.2.2 DC Power Connector

DC power connector (J5) is a 6 pin AMP Mate-N-Lok connector P/N 1-380999-0 mounted on the solder side of the PCB (Refer to Figure 2-8). The recommended mating connector (P5) is AMP P/N 1-480270 utilizing AMP pins P/N 60619-1. J5 pins are labeled on J5 connector.

CAUTION: Before applying DC power insure correct -5/-15 jumper configuration See paragraph 2.4.2.

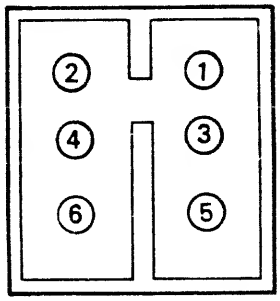


FIGURE 2-8
J5 CONNECTOR

2.2.3 Interface Connectors

Two interface cable connections are required by the Series 2000; a control cable (J1) and a signal or data cable (J2). Details of the control and data signals required can be found in Section 3 INTERFACE.

Connection to J1 is through a 50 pin PCB edge connector. Connector dimensions are shown in Figure 2-9. The pins are numbered 1 through 50 with the even pins located on the component side of the PCB and odd pins located on the solder side of the PCB. Pin 2 is located on the end of the PCB connector closest to the J2 connector and is labeled. A key slot is provided between pins 4 and 6. The recommended mating connector for P1 is Scotchflex ribbon connector P/N 3415-0001.

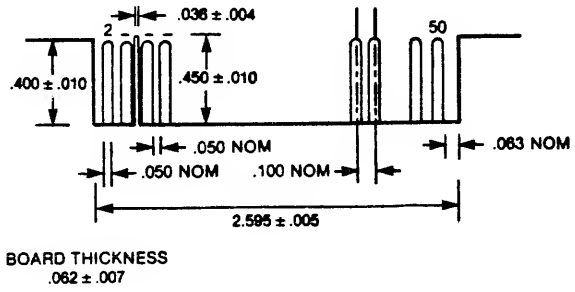


FIGURE 2-9
J1 CONNECTOR

Connection to J2 is through a 20 pin PCB edge connector. Connector dimensions are shown in Figure 2-10. The pins are numbered 1 through 20 with the even pins located on the component side of the PCB. The recommended mating connector for P2 is Scotchflex ribbon connector P/N 3461-0001. A key slot is provided between pins 4 and 6.

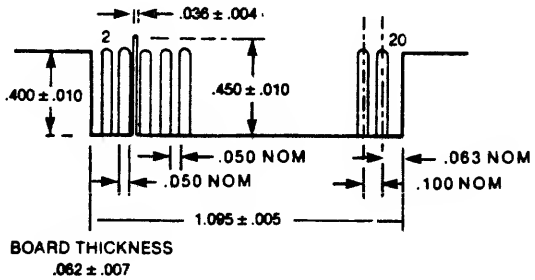


FIGURE 2-10
J2 CONNECTOR

2.3 VENTILATION

All versions of the Series 2000 operate without a cooling fan provided the ambient air temperature does not exceed 115°F (46°C). Any user designed cabinet should provide adequate air circulation so that this maximum temperature is not exceeded.

2.4 OPERATION

2.4.1 General Procedures

Functions performed by the operator vary depending on the user system in which the drive is installed. The information in this subsection describes those functions that may be performed by an operator. These are: minus power selection, drive selection, control cable termination, and Re-zero selection. Figure 2-11 shows the location of the selection jumpers and cable terminator on the Series 2000 drive.

2.4.2 Minus Power Selelction

The Series 2000 requires -5VDC but will regulate greater negative voltages between -7VDC and -16VDC. A jumper plug is supplied at PCB location H9 (See Figure 2-11) that allows the user to select which negative voltage will be supplied to the drive. The drive is shipped with the jumper in the -15VDC position. If the user is supplying -5VDC, the jumper should be moved to the -5V position.

CAUTION

Damage to components that use -5VDC can occur if the jumper is in the -5V position and greater negative voltages are applied to the drive.

2.4.3 Drive Select

Five jumpers are provided for logical drive number assignment. DS1, DS2, DS3, DS4 cause the drive to be selected when the active drive select line matches the installed jumper. Jumper A, when installed, causes the drive to be selected constantly. The Quantum part number for the jumper plug is 22-10036.

2.4.4 Control Cable Termination

If the Series 2000 is the last drive at the end of the control signal cable, a 220/330 ohm terminator pack must be installed at PCB location J6. The terminator must be removed from J6 if the drive is not at the end of a string of drives. The Quantum part number for the terminator pack is 13-12302.

2.4.5 Re-zero Select

The Series 2000 can be re-calibrated to track 000 by driving a single control line. This re-zero function will also cause the drive to initialize its thermal compensation bytes. If use of this re-zero function is desired, jumper C at PCB location J5 should be installed, this allows J1 pin 6 to be used to initiate the rezero function.

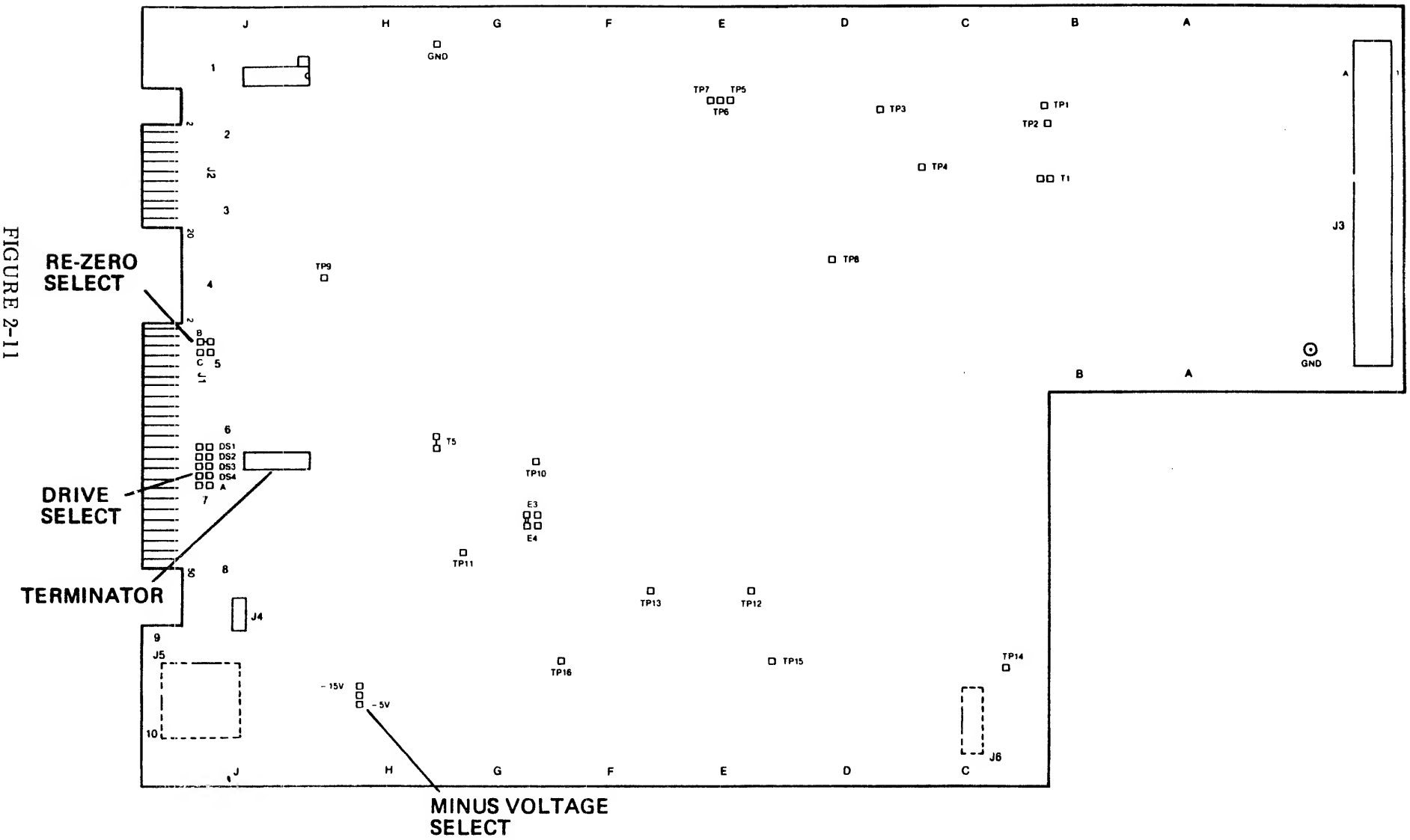


FIGURE 2-11
SERIES 2000 JUMPER OPTIONS

SECTION 3

INTERFACE

3.1 INTRODUCTION

The Series 2000 has two interface connectors: one for control signals which are TTL in nature and one for data transfer signals which are differential in nature. This section is devoted to defining the signals, timing requirements and interface cables associated with these two interface connectors. The characteristics of the receiver/driver combinations used is also discussed. Figure 3-1 shows the location of these two connectors.

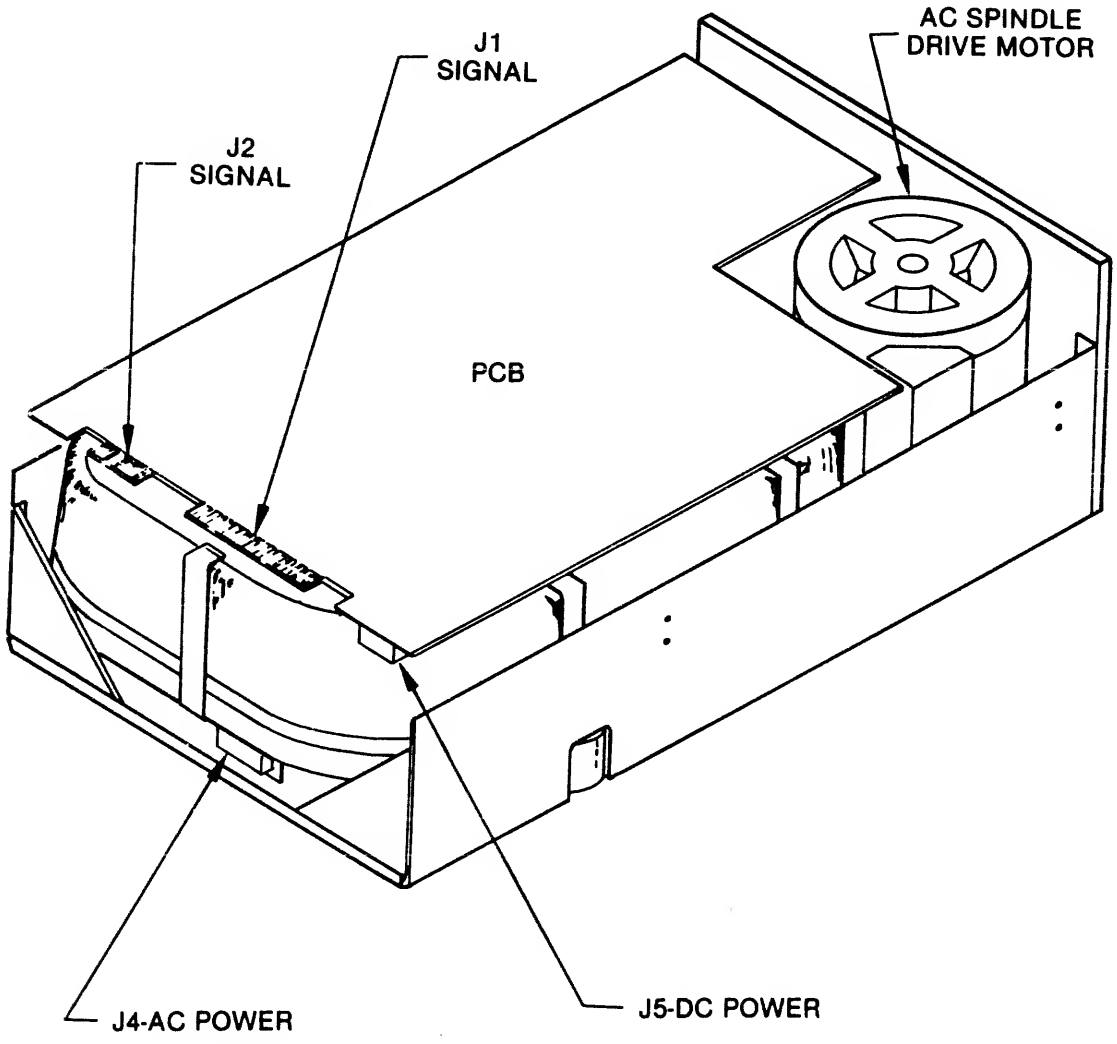


FIGURE 3-1
SERIES 2000 INTERFACE CONNECTIONS

3.2 CONTROL SIGNAL INTERFACE

3.2.1 General Description

The control signals are both input, those originating external to the drive and output, those originating within the drive. The control signals could also be divided into two types: those intended to be multiplexed in a multi-drive system and those intended to do the multiplexing. The control signals that do the multiplexing are DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3, and DRIVE SELECT 4 which are input signals. The multiplexed signals are: STEP, DIRECTION, HEAD SELECT 2^0, HEAD SELECT 2^1, HEAD SELECT 2^2, WRITE GATE, REDUCE WRITE CURRENT, and REZERO input signals, TRACK 000, INDEX, READY, WRITE FAULT and SEEK COMPLETE output signals. Up to four drives may be connected in a daisy-chain configuration using a single control signal cable. The last drive in the chain requires the terminator to the intalled at PCB location J6.

The input lines have the following electrical specifications:

Logic "0" = True = 0.0 VDC to 0.4 VDC at I in = 40 MA (MAX) = LO
Logic "1" = False = 2.5 VDC to 5.25 VDC at I in = 0 MA (OPEN) = HI

The output lines are driven with a TTL open collector output stage capable of sinking a maximum of 40 MA at the logic "0" or TRUE state with a maximum voltage of 0.4 VDC measured at the driver. When the line driver is in the logic "1" or FALSE state the driver transistor is off and the collector cutoff current is 250 microamperes.

3.2.2 Driver/Receiver

Figure 3-2 shows the recommended control signal driver/receiver combination. The maximum recommended cable length is 20 feet (6m). The pin designations of the control cable are shown on figure 3-3.

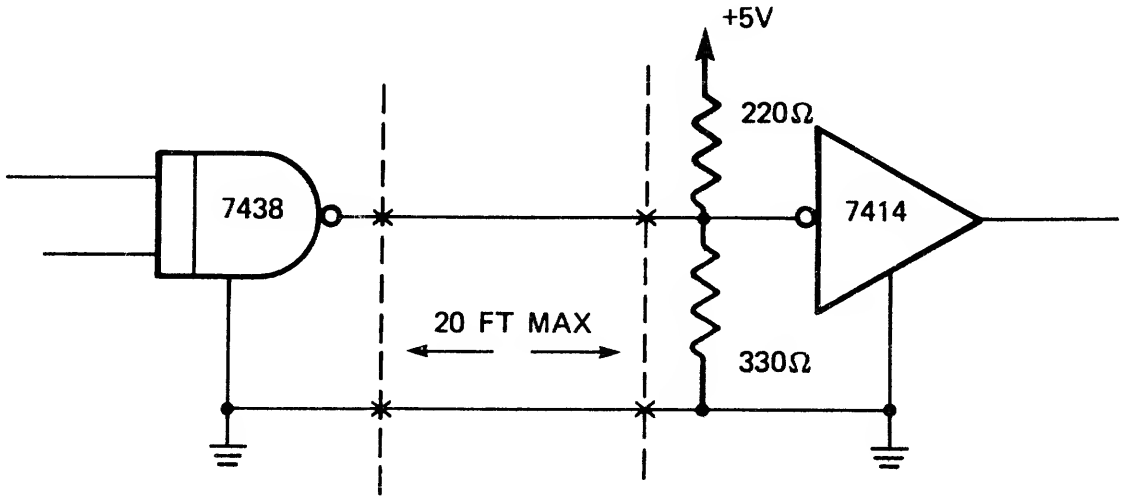


FIGURE 3-2
CONTROL SIGNAL DRIVER/RECEIVER

Ground Return	Signal Pin	Signal Name
1	2	−Reduced Write Current
3	4	−Head Select 2^2
5	6	−Rezero (Jumperable Option)
7	8	−Seek Complete
9	10	−NA
11	12	−NA
13	14	−Head Select 2^0
15	16	−NA
17	18	−Head Select 2^1
19	20	−Index
21	22	−Ready
23	24	−NA
25	26	−Drive Select 1
27	28	−Drive Select 2
29	30	−Drive Select 3
31	32	−Drive Select 4
33	34	−Direction In
35	36	−Step
37	38	−NA
39	40	−Write Gate
41	42	−Track 000
43	44	−Write Fault
45	46	−NA
47	48	−NA
49	50	−NA

FIGURE 3-3
CONTROL CABLE PIN DESIGNATIONS

3.2.3 Control Signal Descriptions

The function of each of the thirteen (13) control signals is described below:

INPUT SIGNALS

- DRIVE SELECT 1, 2, 3 ,or 4 - A LO level on this line logically connects the drive to the control lines. Only one drive select line may be active at a time and it will select the drive which has the matching drive select jumper installed.

- DIRECTION IN - A LO level on this line defines the R/W head motion as in or toward the center of the disk (away from track 000). Motion occurs with receipt of a step pulse. A HI level on this line defines the R/W head motion as out or toward the edge of the disk (toward track 000).

- STEP - A LO pulse, of at least 1.0 usec duration, on this line will cause the R/W head to move in the direction defined by the DIRECTION IN line. If STEP pulses occur at a rate equal to or greater than 1.5 MS between pulses the heads will move at the rate of the incoming steps (normal step mode). If the incoming step pulse rate is equal to or less than 600 usec between pulses, the pulses are buffered into a counter and motion occurs after the last step pulse is received (burst mode). See Figures 3-4 and 3-5 for Step Timing.

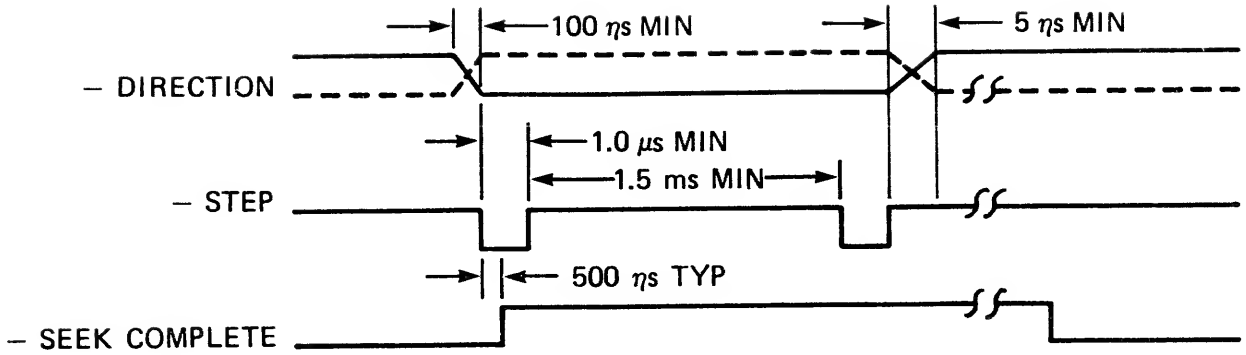


FIGURE 3-4
NORMAL STEP MODE TIMING

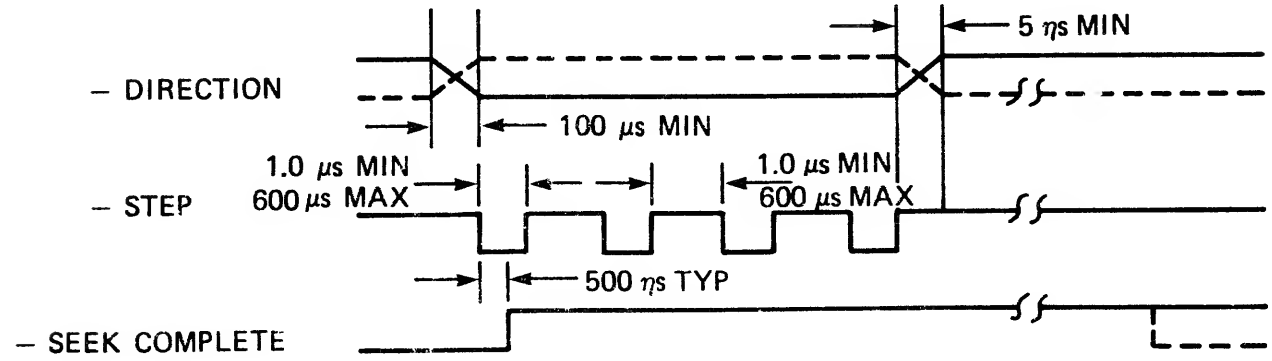


FIGURE 3-5
BUFFERED STEP MODE TIMING

- HEAD SELECT 2^0, 2^1, and 2^2 - These three lines provide a binary code to select one of the heads. 2^0 is the least signficant bit and the heads are numbered 0 through 7. When all lines are LO head 7 is selected. Conversely, if all lines are HI, head 0 is selected.
- WRITE GATE - A LO level enables write data to be written on the disk.
- REDUCE WRITE CURRENT - A LO level on this line selects a lower level of write current to be used when writing. It is recommended that the lower level be used when writing on cylinders 256 through 511.
- RE-ZERO - When this feature is enabled by installing jumper "C" on the control PCB and a LO pulse of at least 50 usec duration occurs on this line the drive will reset the microprocessor and recalibrate to cylinder 000.

OUTPUT SIGNALS

- TRACK 000 - A LO level on this line indicates the R/W heads are positioned at cylinder 000 (the outermost cylinder).

- INDEX - A LO pulse, of 10 usec duration on this line indicates the beginning of a track. The leading edge of this pulse must be used for all timing requirements. The pulse occurs once each revolution or every 20 msec. Figure 3-6 illustrates the index timing.

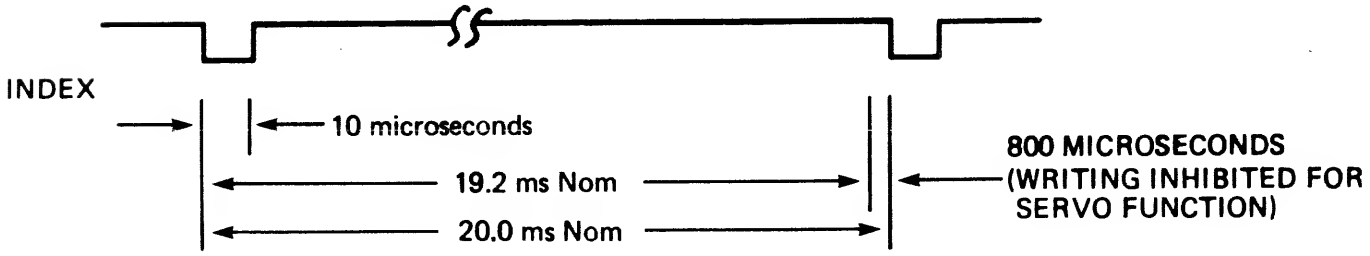


FIGURE 3-6
INDEX TIMING

- READY - A LO level on this line indicates the drive is up to speed and the interface signals are valid. When READY and SEEK COMPLETE are true, the drive is ready to read, write or seek.

- WRITE FAULT - A LO level on this line indicates write current is flowing in the selected head and WRITE GATE is not true (HI). Write Fault may be reset by: deselecting the drive, driving the Re-zero line, or cycling the DC power off then on.

- SEEK COMPLETE - A LO level on this line indicates the R/W heads have settled on a cylinder and a read, write or another seek may take place.

Figure 3-7 shows the general timing relationships between some of the control signals found in the Series 2000.

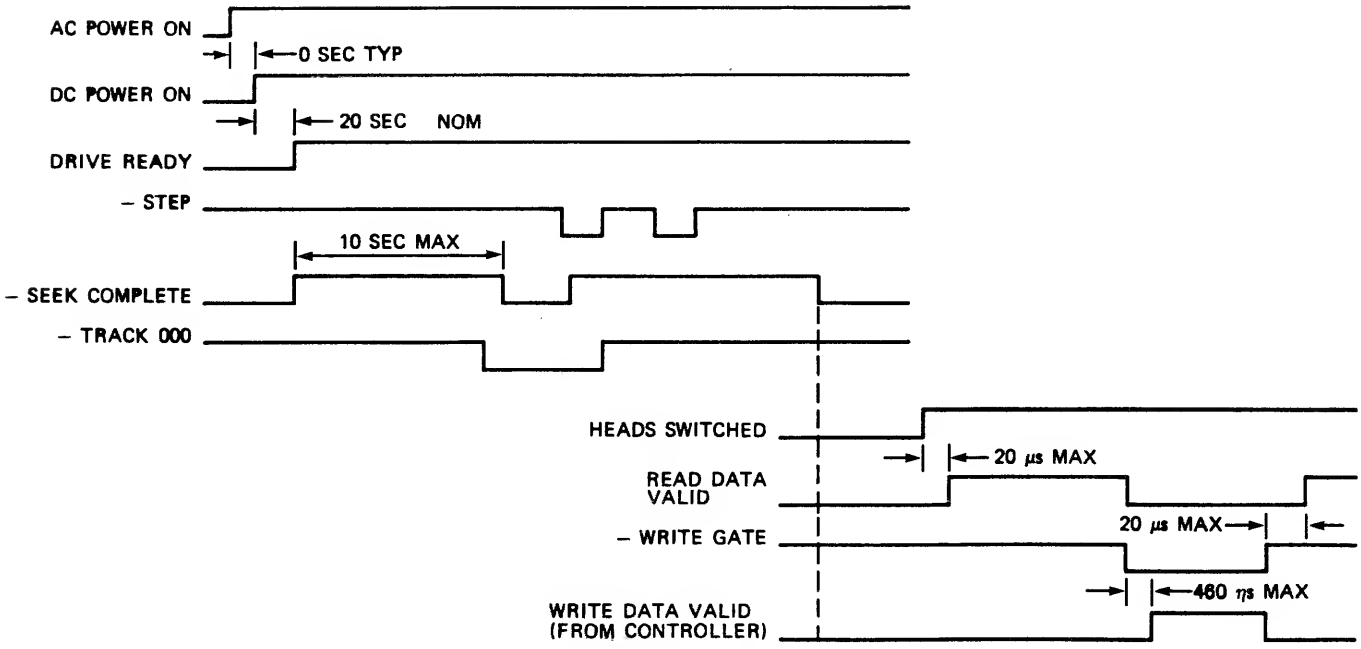


FIGURE 3-7
GENERAL CONTROL TIMING REQUIREMENTS

3.3 DATA INTERFACE

3.3.1 General Description

There are three signals on the data interface cable and they are not multiplexed. Two of the signals are differential in nature, MFM WRITE DATA (input) and MFM READ DATA (output); the third, DRIVE SELECTED, is a TTL open collector output. The differential signals have the following electrical characteristics.

Driver output current is 15 ma maximum on the driven line and 100 ua on the non-driven line. The output voltage range is -3 to +10 VDC. The receiver input voltage is -5 V to +5 VDC on either line. The circuit will detect a differential voltage of 25 MV. The maximum input current is -10 to 75 ma. The TTL DRIVE SELECTED signal has the same electrical characteristics as the output lines described in paragraph 3.2.2. Figure 3-9 shows the pin designations of the data signals.

3.3.2 Driver/Receiver

Figure 3-8 shows the recommended differential data signal driver/receiver combination. See Figure 3-2 for the DRIVE SELECTED driver/receiver combination.
The maximum recommended cable length is 20 feet (6m).

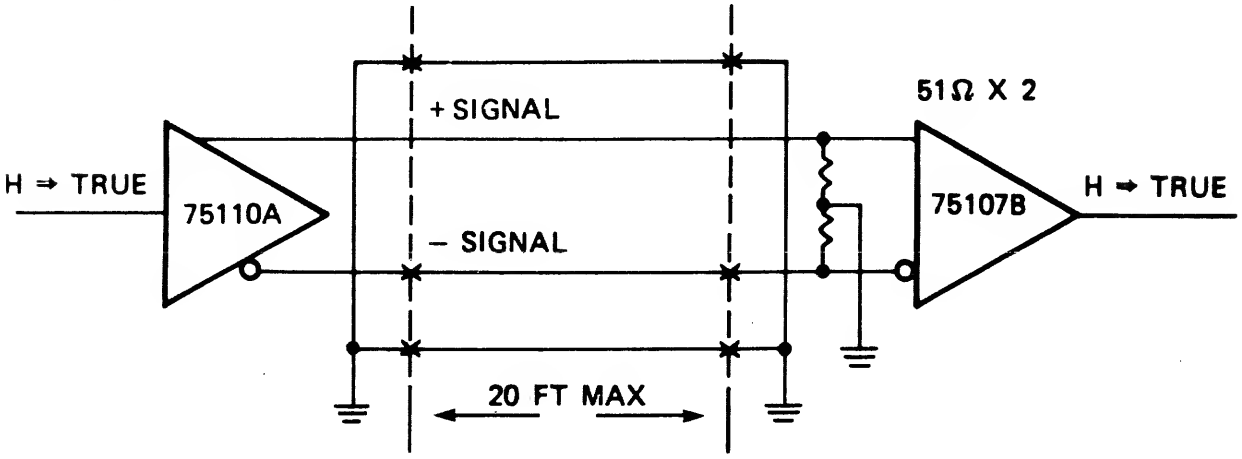


FIGURE 3-8
DATA SIGNAL DRIVER/RECEIVER

Ground Return	Signal Pin	Signal Name
2	1	– Drive Selected
4	3	Seek Complete (Jumperable Option)
6	5	Spare
	7	Spare
8		GND
	9	+ Timing Clk
	10	– Timing Clk
11		GND
12		GND
	13	+ MFM Write Data
	14	– MFM Write Data
15		GND
16		GND
	17	+ MFM Read Data
	18	– MFM Read Data
19		GND
20		GND

FIGURE 3-9
DATA CABLE PIN DESIGNATIONS

3.3.3 Data Signal Descriptions

The function of each of the three (3) data signals is described below:

- MFM WRITE DATA - Provided there is a LO level on the WRITE GATE control line the transition of the +MFM WRITE DATA line more positive than the -MFM WRITE DATA line will cause a flux reversal to be written on the disk. During read operations the +MFM WRITE DATA line must be held more negative than the -MFM WRITE DATA line. Figure 3-10 shows the write data timing.

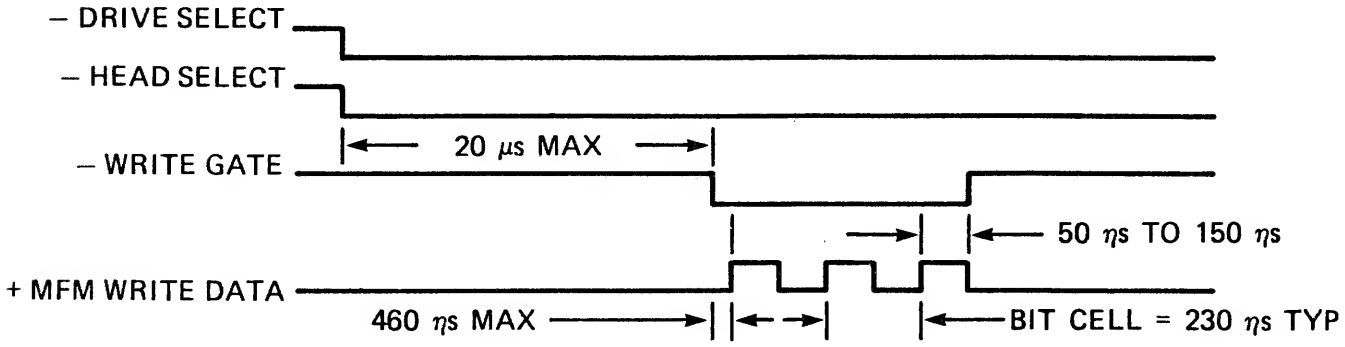


FIGURE 3-10
MFM WRITE DATA TIMING

- MFM READ DATA - Provided there is a HI level on the WRITE GATE control line the transition of the +MFM READ DATA line more positive than the -MFM READ DATA line indicates a flux reversal was detected on the track. Figure 3-11 shows the read data timing.

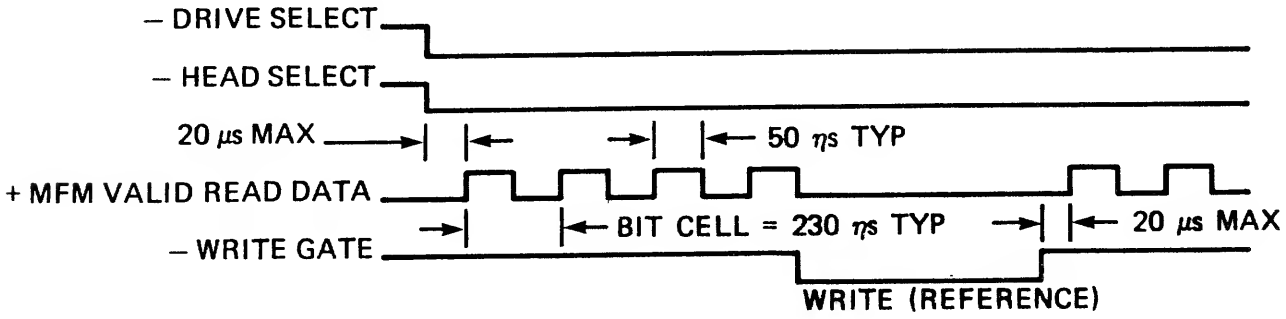


FIGURE 3-11
MFM READ DATA TIMING

- DRIVE SELECTED - This open collector line will go to a LO level when this drive is selected by the appropriate drive select line.

SECTION 4

PRINCIPLES OF OPERATION

4.1 SERIES 2000 BLOCK DIAGRAM

The block diagram shown on Figure 4-1 is representative of all four models of the Series 2000 disk drive. AC power, either 110 VAC or 220 VAC, is used to supply power to the AC spindle drive motor. The spindle is driven from this motor by a belt and pulley arrangement. There is a belt/pulley set for each of the two AC frequencies, 50 HZ and 60 HZ. These interchangeable belt/pulley sets allow the spindle to rotate the disk(s) at 3000 RPM for either frequency. Below the disk(s) in the base casting is the index transducer, a magnetic pickup that senses a metal pin pressed in the disk mounting hub. The pulse generated is the index pulse that provides beginning of track timing to the host system via the drive control electronics PCBA. The head stack assembly is mounted to the rotor of the proprietary rotary positioner assembly. The positioner motor is driven from circuitry on the control PCBA via power drivers on the heat sink. Track position signals are obtained from an optical encoder and scale assembly via the transducer PCBA. Read/write signals are obtained from or written to the disk via the heads and the head switching matrix on the transducer PCB. The drive control PCBA contains the electronics for read/write detection and drive, servo position decoding, positioner drive, and the microprocessor that controls these functions.

4.2 SERIES 2000 DRIVE MECHANISM

The drive mechanism consists of the mechanical subassemblies of the drive which are sealed under a plastic bubble. None of these have adjustments nor are they field repairable. Their functions are described here to give the reader a more thorough understanding of the Series 2000.

4.2.1 Base Casting Assembly

The base casting is a single piece cast aluminum alloy which provides a mounting surface for the rest of the drive mechanism. It has three machined holes used to mount the spindle assembly, the positioner assembly and the index transducer. The outside top edge is flat to insure an air tight seal with the bubble cover when installed. Surfaces are provided for mounting the optical encoder, transducer PCB and the upper magnet plate for the positioner motor. Mounting holes are also provided, outside the bubble area, for the AC drive motor, and belt guard spindle ground assembly.

4.2.2 Disk Stack Assembly

The disk stack assembly consists of the spindle bearing assembly, disk mounting hub, disks, disk spacers, disk clamp, drive pulley, spindle grounding system, and ferrous exclusion seal. The bearing assembly is bonded in place and a ferrofluid magnetic seal is applied at the top of the assembly. This seal prevents outside air from entering the drive through the bearing bore or along the bearing shaft. The disk mounting hub has an iron pin pressed into its perimeter that is sensed by the index transducer to provide raw index. Depending on the drive capacity, one to four disks and spacers are placed on the hub and clamped in place. The disks are an aluminum alloy with a magnetic oxide coating. The oxide coating is polished and lubricated. The lubrication prevents head and media wear when the heads are in contact with the disk surface, which only occurs outside the data area and the disks are not rotating.

The drive pulley is mounted on the bottom of the spindle bearing assembly and provides a coupling surface for the drive belt and AC Drive motor. The spindle grounding system consists of a carbon button bonded to the spindle screw, and a spring contact on the belt guard.

4.2.3 AC Drive Motor Assembly

The Series 2000 spindle is driven by an induction AC motor and belt/pulley combination. Two motors are available, one for 110 VAC operation and another for 220 VAC operation, both motors will operate at either 50 or 60 HZ. However, since the 50 HZ input will result in a slower motor rotational speed than the 60 HZ input, different size pulleys and belts are used to set the spindle rotational speed at 3000 RPM regardless of input frequency. Changing the Series 2000 from one frequency or voltage to the other is described in Section 5, paragraph 5 of this manual. The motor capacitor and AC input connector are both part of the AC motor assembly. The capacitor is used to provide the necessary phase shift to get the motor started and run at the correct speed. The motor is mounted on the base casting by three bolts and is isolated from direct contact with the base casting with plastic washers. This isolation provides AC ground isolation and prevents excessive motor vibrations from being mechanically coupled into the drive base. Mounted to the motor shaft is the drive pulley whose size is dependent on AC line frequency. (The 50 HZ pulley is larger than the 60 HZ pulley).

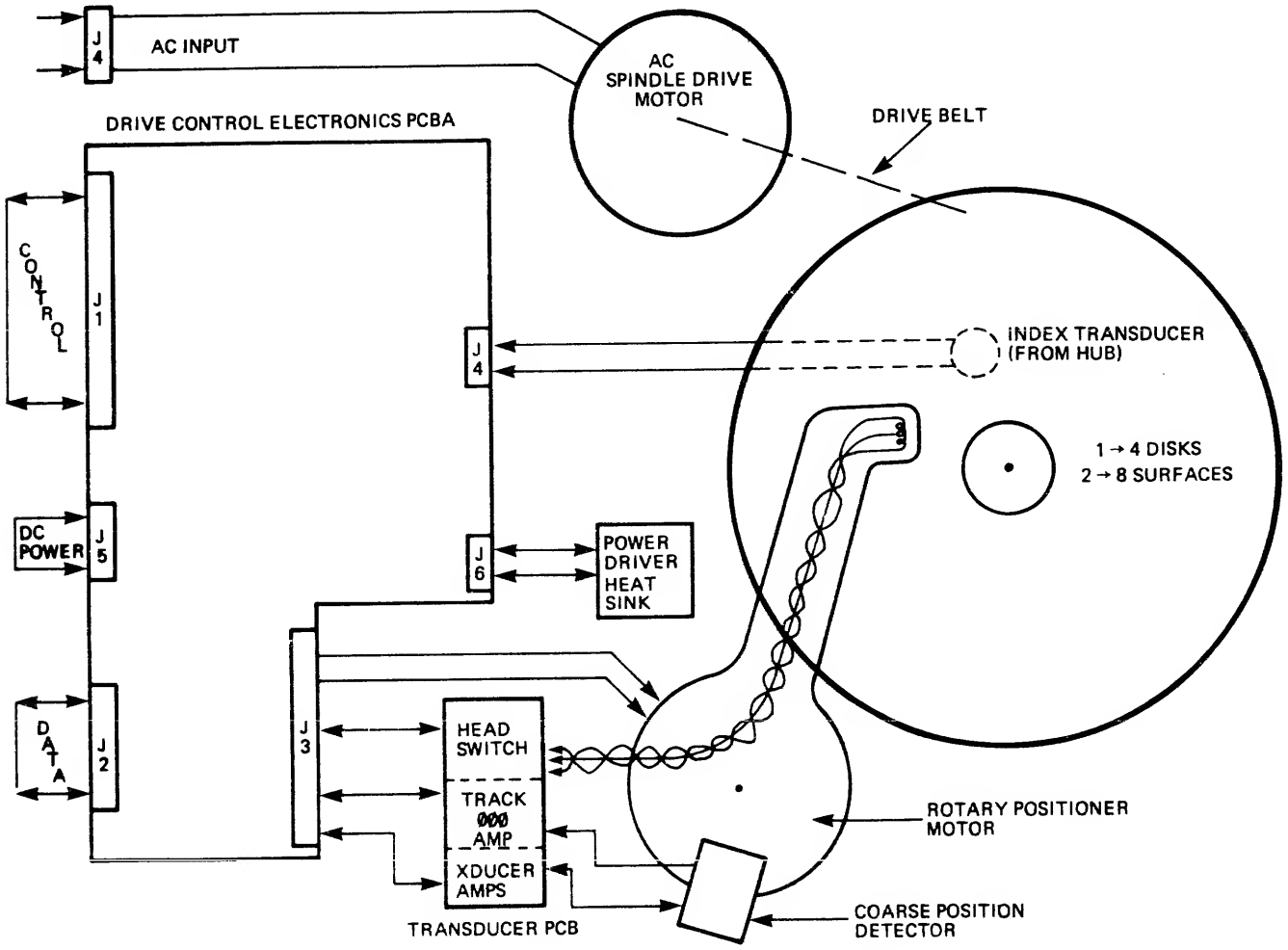


FIGURE 4-1
Series 2000 BLOCK DIAGRAM

4.2.4 Rotary Positioner Assembly

The positioner used in the Series 2000 is a design proprietary to Quantum consisting of the upper and lower magnet plates, a rotary dual phase coil, a head stack mounting hub, a magnet ring and a bearing shaft. The magnet is composed of six alternating poles bonded to the lower magnet plate which in turn is bolted to the base casting. The rotor and hub are bonded together and the bearings and shaft are bonded into the hub. This entire assembly is then assembled into the base casting where the bearing shaft is bonded into the casting. The shaft/casting bond provides not only mounting rigidity, but also forms an air tight seal between the shaft and mounting bore. This is also true for the bearing to shaft bond and bearing to hub bond. The upper magnet plate is placed over the rotor/hub assembly to provide a return path for the magnetic field. This design allows the mass center of the head stack to be placed at the hub so that bearing wear is minimized and all motor power is converted to torque. Mounted to the upper magnet plate is the crash stop which prevents the heads from being driven into the spindle or off the disk surface.

4.2.5 Head Stack Assembly

The head stack assembly consists of the heads, head arms and counter balances, in addition the optical scale is bonded to the lower head arm. The counter balances are castings whose shape and weight are designed to insure that the mass center of the entire stack is at the center of the mounting hub. The lower counter balance is slightly different than the others in that it holds the rubber crash stop bumper. The heads are Winchester slider type with a .0022" track width mounted to spring steel flexures which are staked to the head arm. The head conductors are routed in plastic guides and tacked in place with an adhesive. All head stack assemblies have an upper and lower head arm assembly and may have up to three dual head arm assemblies.

The lower head arm assembly is different from the others as it has the mounting pads for the optical scale. This scale is used in conjunction with the optical encoder and transducer PCBA to generate the track position signals.

4.2.6 OPTICAL ENCODER

The optical encoder is mounted on a shaft pressed and bonded into the base casting. The assembly consists of a housing, an infrared light emitting diode , an optical reticle, a multi-cell photo diode matrix, and a flex circuit connection to the transducer PCBA.

The infrared LED is mounted in the lower half of the housing. This allows the optical scale on the lower arm to move between the infrared LED and the upper half of the housing which contains the reticle and photo cells. The reticle masks the six photo cells so that each cell only receives light through a specific portion of the movable scale. Both the clearance and angular position of reticle and scale are precision adjustments that are made when the drive is manufactured. The electrical signals from the photo cells are carried to the transducer PCBA via a copper/kapton flex circuit. These signals are more fully explained in paragraph 4.3 of this section.

4.2.7 Air Filtration

The Series 2000 is a Winchester type drive, and as such the heads fly very close to the media surface. The nominal flying height is 18 micro inches or roughly 1600 times smaller than the period at the end of this sentence.

It is absolutely essential that the air circulating within the drive is kept clean of particles. This task is accomplished by sealing the drive in a plastic bubble and using the rotating disks as an air pump to force the air through two filters. Figure 4-2 shows the air flow in the enclosed area of the drive. The lowest pressure area within the drive is located at the top in the center of the spindle. A 0.3 micron breather filter is bonded in this area of the bubble. This filter allows outside air into the bubble enclosure to equalize internal and external pressures. The highest pressure area within the drive is located at the outer edge of the lowest disk. Bonded in the base casting at this location is another 0.3 micron filter called the circulation filter. Air constantly pumped into the top of this filter is filtered and exits from the bottom into a channel cut in the base casting. This channel extends from the filter to a location close to the spindle where pressure is lower than that at the top of the filter. This insures a continuous flow of filtered air as soon as the disks start to rotate. Due to the stringent cleanliness required, the bubble and or seals should not be tampered with in normal environments. Optional Section 8 of this manual describes the required environment and procedures that should be strictly adhered to prior to attempting any sub-bubble repairs.

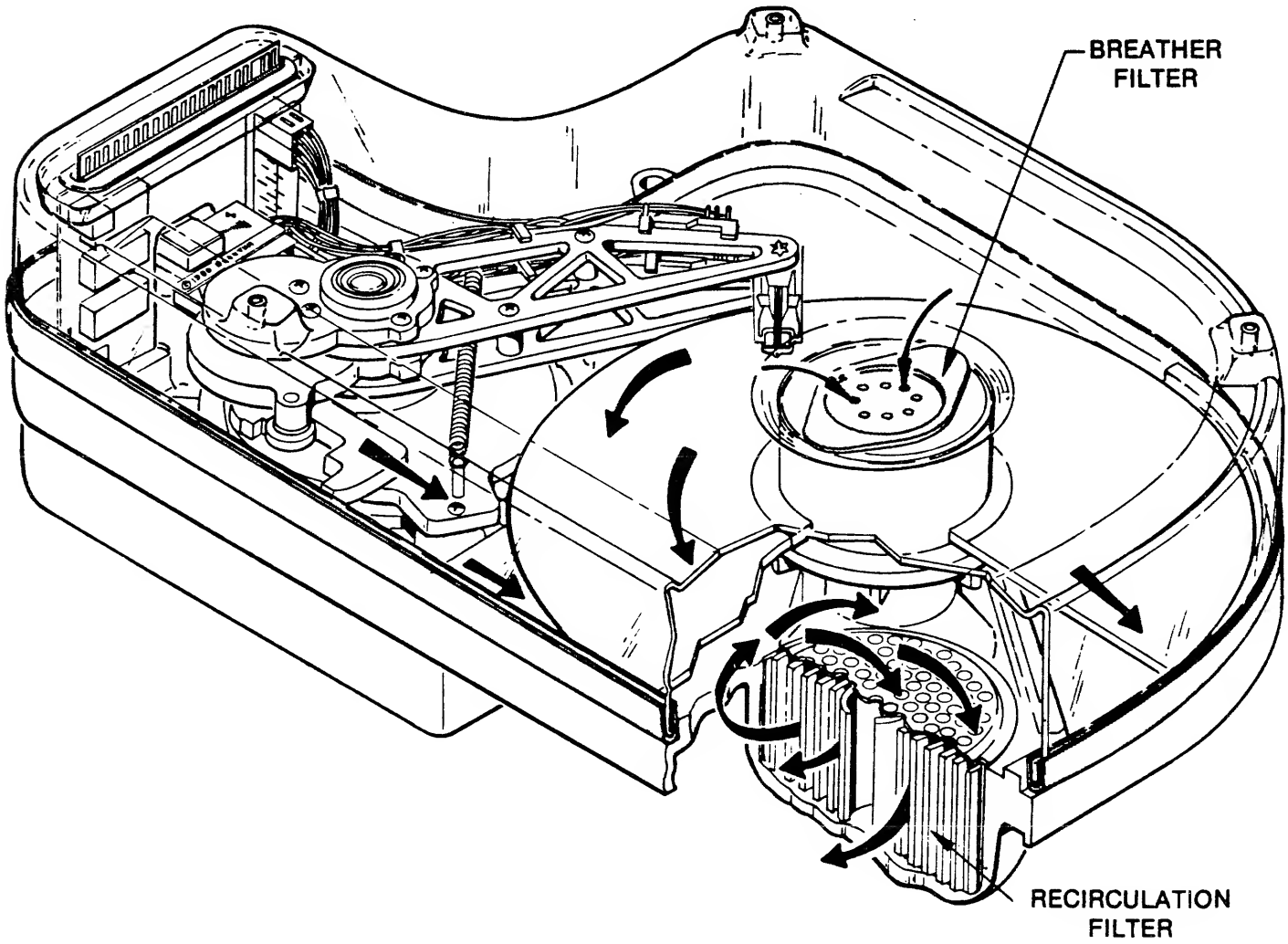


FIGURE 4-2
AIR FILTRATION SYSTEM

4.3 SERIES 2000 DRIVE ELECTRONICS

4.3.1 General Discussion

This section describes in detail the operation and functions performed by the Series 2000 electronics. Simplified schematics are used to assist the reader in understanding the various functions. All component references are the same as those used on the drive schematics included in Section 6. Location references used refer to page locations on these schematics. Figure 4-3 is a functional block diagram of the Series 2000 drive electronics. Each of the functional areas shown is discussed in detail in the following paragraphs. The drive electronics contains the following circuitry:

- Interface Buffers - These drivers and receivers buffer the control and data signals between the drive and the drive controller. The function of the various interface signals is described in Section 3.

- D.C. Power Circuits - This circuitry is used to provide power decoupling and regulation as well as the power up reset signal.

- Index and Timing Generator - Using the mechanical index as a reference input a time slot for reading the servo data is generated followed by an index pulse to the user interface.

- Read/Write Electronics - This circuitry provides the write current to record data and the circuits to detect recorded data.

- Transducer PCBA - This PCBA contains the head switching matrix, and the circuits used to generate track position signals from the signals provided by the scale and optical encoder.

- Coarse Position Detection - This circuitry uses the output of the transducer PCBA to generate track quadrature signals used to position the head stack on a track.

- Fine Position Detection - By using the signals from the factory recorded servo bursts, this circuitry provides fine position correction for thermal compensation.

- Actuator Drive Circuits - This circuitry provides the power to drive the actuator.

- Microprocessor - This single chip processor controls the drive during its various modes of operation.

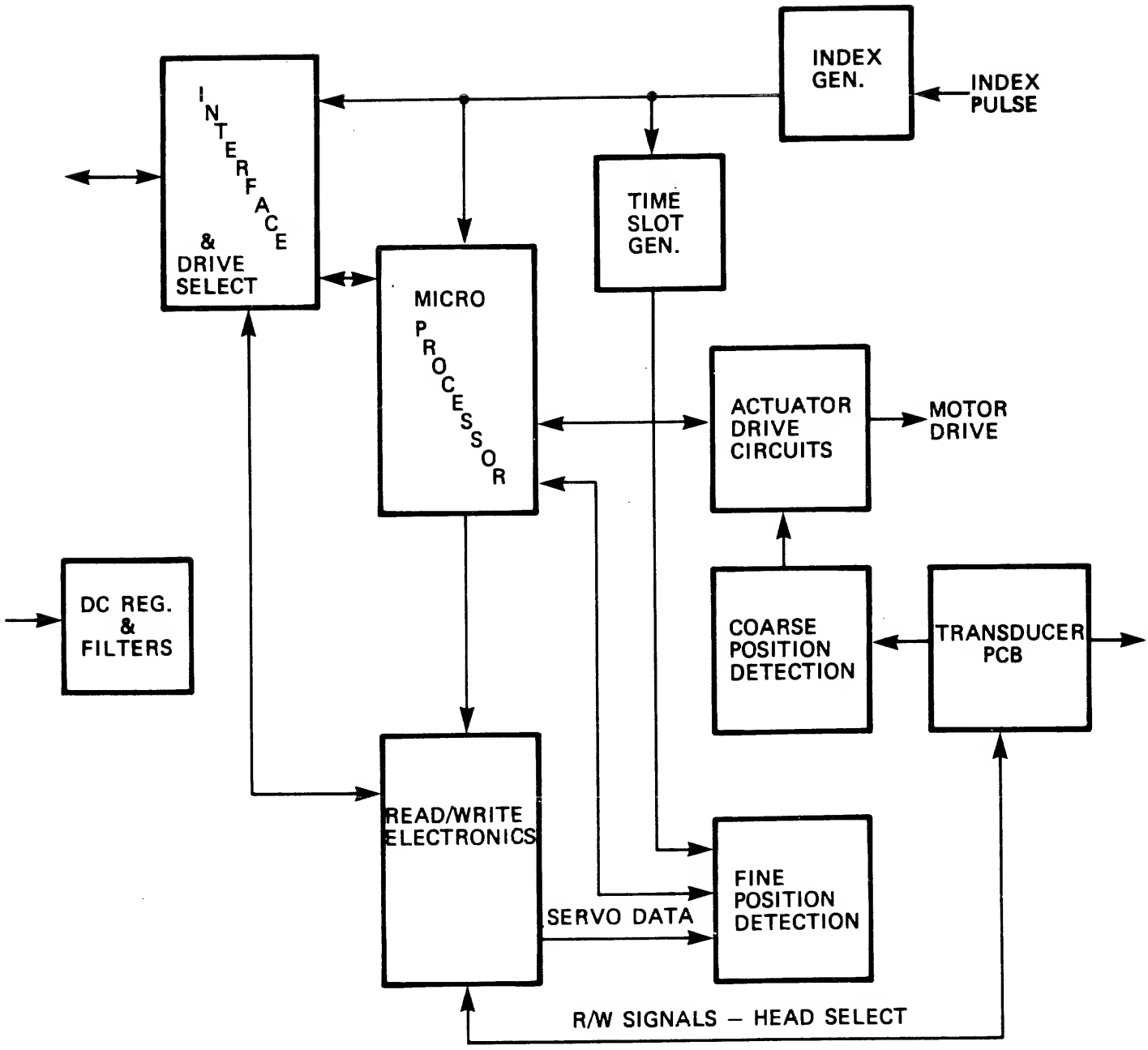


FIGURE 4-3
DRIVE ELECRONICS BLOCK DIAGRAM

4.3.2 Transducer Board, PN80-20010, REV B

4.3.2.1 Block Diagram

Figure 4-4 is a functional block diagram of the transducer PCBA. The board contains: the diodes used for head switching, a through bubble connector (for the head signals, actuator drive signals and actuator position signals), the amplifiers and comparators used to detect the encoder photo cell outputs, and the AGC amplifier used to control the infrared LED drive current.

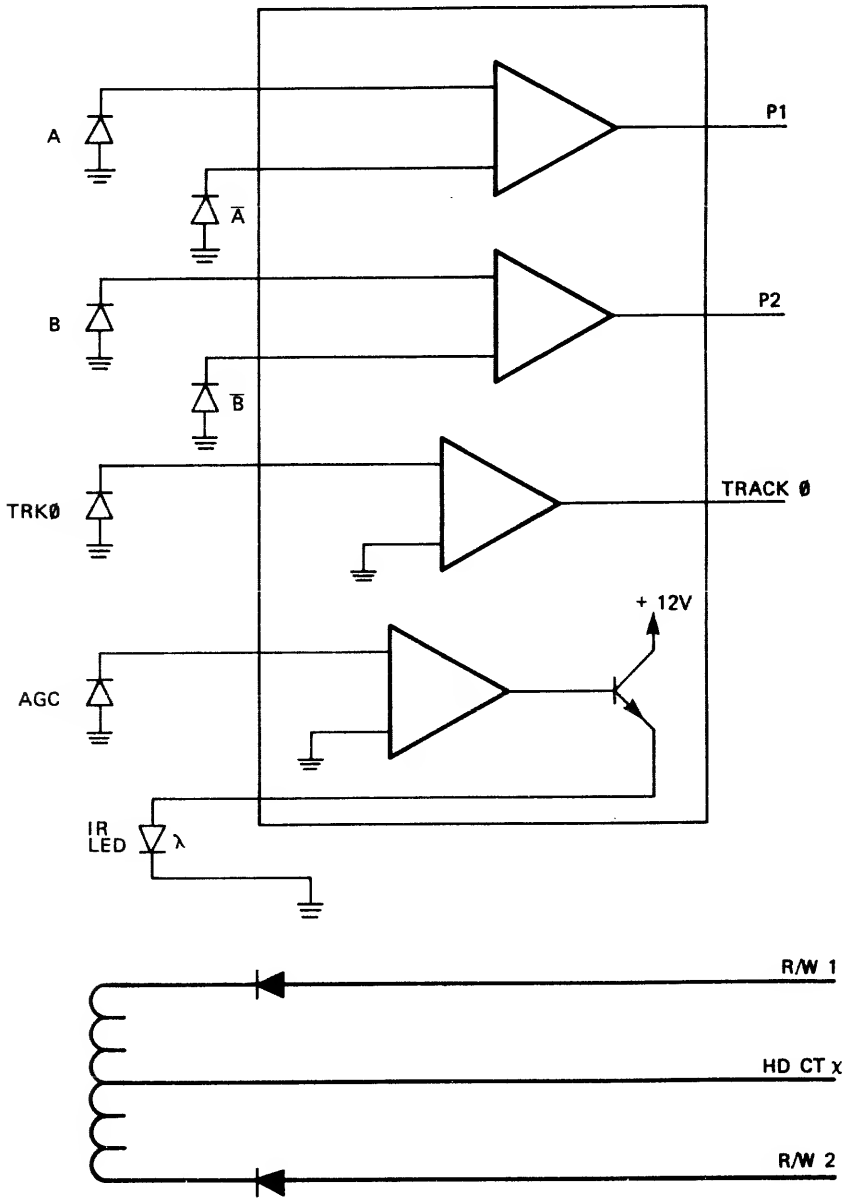


FIGURE 4-4
TRANSDUCER PCBA BLOCK DIAGRAM

4.3.2.2 Head Switching Matrix

Figure 4-5 is a simplified schematic of the head switching diode matrix for two heads. Refer to Section 6, Figure 6 for the actual matrix used.

Diodes CR7, CR8, CR15 and CR16 are part of the head switch matrix. When the head switch IC grounds the head centertap (HDCT0 - 7) the selected head is connected to the Read/Write circuits via one of the diode pairs. None of the other diode pairs is forward biased, therefore, the other heads are isolated from the selected head. Diodes CR6 through CR9 are part of the Read/Write circuits and are used to isolate the Read and Write circuits from each other. See paragraphs 4.3.3.6 and 7.

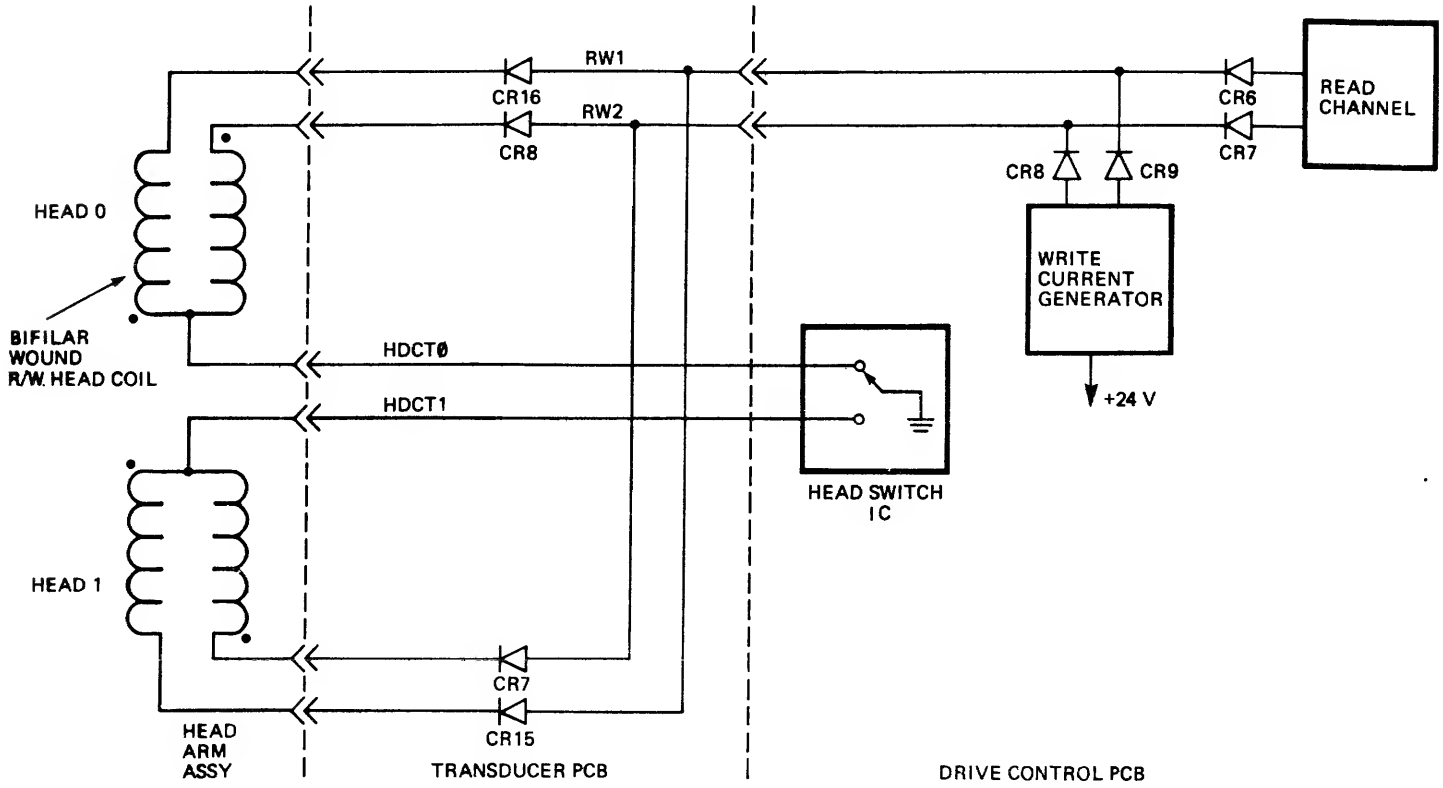


FIGURE 4-5
HEAD SWITCHING MATRIX

4.3.2.3 AGC Circuit

Paragraph 4.2.6 described the mechanical operation of the transducer scale reticle and photo cell. The AGC window in the reticle provides its photo cell with a large view of the scale in order to sense an average of the amount of light striking any of the other cells. Figure 4-6 is a simplified schematic of the AGC circuit. The actual circuit is in Section 6, on page 6-8

Amplifier U1 drives the base of Q1 which provides the current for the infrared LED. R1 is adjusted at the factory to provide the proper signal amplitude out of the track position amplifiers. Once R1 is adjusted the amount of light produced by the LED will depend on the amount of light seen by the AGC photo diode. If the photo diode output decreases (less light seen) amplifier U1 output goes more positive, Q1 conducts harder, passing more current to the LED which outputs more light until the circuit stabilizes again. In this way the signal amplitude of the other photo diodes is held constant over the entire scale, compensating for aging and variations in temperature and voltage.

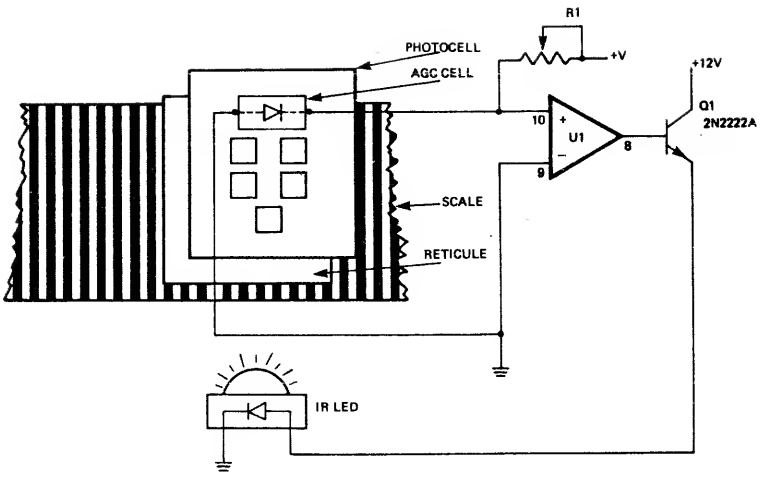


FIGURE 4-6
SIMPLIFIED AGC CIRCUIT

4.3.2.4 Track 000

Refer to Figure 6-6 B4. The Track 000 photo cell is illuminated over the entire scale except when the scale is positioned at track 000. Here the scale blocks the light to the cell. When the cell is illuminated it outputs a HI level causing U1-14 to also output a HI level. When the dark area on the scale blocks the light at Track 000 the cell output switches LO causing the output of U1-14 to switch LO providing the Track 000 signal to the drive electronics.

4.3.2.5 P1 and P2 Generation

The P1 and P2 signals are the signals used to determine coarse track position. As seen on the simplified schematic in Figure 4-7(a) one pair of photo cells (connected to comparator A) are in opposite states. The cell with no light outputs minimum voltage to the inverting input and the cell with maximum light outputs maximum voltage to the non-inverting input. With these inputs comparator A outputs maximum positive voltage at P1. On the other hand the cells connected to comparator B see equal light and therefore output equal voltages to both inputs of comparator B this results in a zero voltage output at P2. Moving the scale to the next state gives the conditions shown in 4-7(b). Here comparator A has equal inputs, hence, zero output at P1. Comparator B has maximum voltage on the non-inverting input and zero voltage on the inverting input resulting in a maximum positive output at P2. Moving the scale again gives the condition shown in 4-7(c). Once again, comparator B sees equal inputs and P2 is zero volts. Comparator A has different inputs, but they are in the opposite state from 4-7(a); here there is maximum voltage at the inverting input and minimum voltage at the non-inverting input. This results in a maximum negative output from comparator A at P1. Figure 4-7(d) shows the last of the four possible conditions. Here we have no output at P1 and maximum negative output at P2. The waveforms shown in 4-7(e) illustrate the outputs from P1 and P2 that would occur with the scale constantly moving in one direction. The scale and reticle are etched in such a way that the zero voltage point of the P1 or P2 waveform is equal to a track center. Therefore, four tracks are located on the disk in the space between the beginning of one scale line and the beginning of the next scale line. This makes the scale position very accurate allowing the embedded servo data to be used only for thermal compensation.

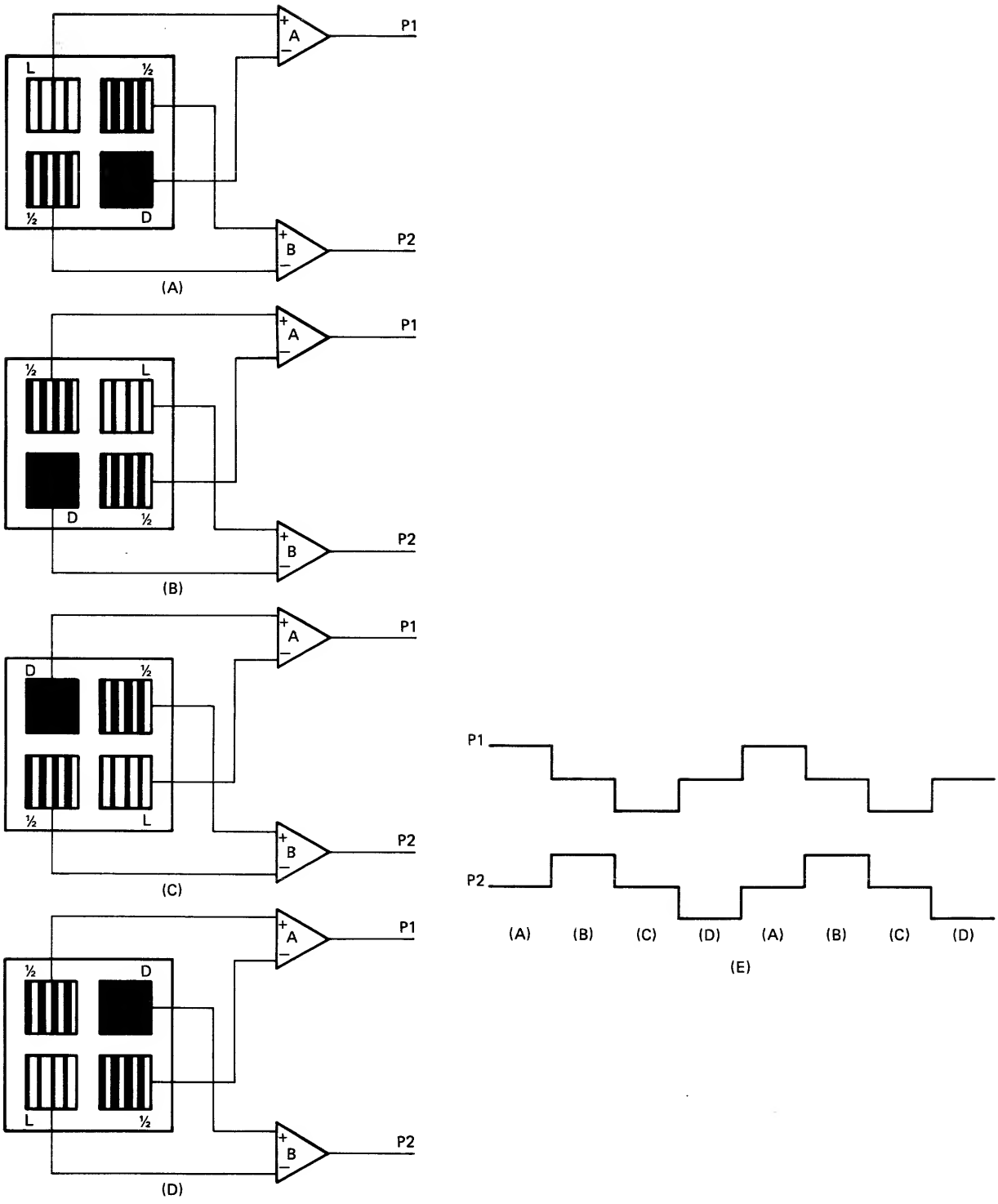


FIGURE 4-7
P1 AND P2 GENERATION

4.3.3 Drive Control Board, PN 80-20000,FAB B, REV P and FAB D, REV N

4.3.3.1 Block Diagram

Figure 4-8 is a functional block diagram of the drive control board. The board is mounted to the top of the drive and connects on one end to the through bubble connector of the transducer PCB. The opposite end of the board provides connectors for the controller data and control signals and DC power, two additional connectors are provided for the index transducer and the actuator power driver transistors.

Applying AC power to the drive causes the AC motor to start the disks rotating this in turn results in the heads lifting off the disk surface and flying above the landing zone. With the application of DC power, a power on reset is generated by the DC power circuits. This resets the microprocessor and all drive logic. The rotational speed of the disks is sensed by the processor and once the disks are up to speed, the processor activates READY and causes the heads to move to track 000. When track 000 is sensed the heads are moved to tracks 508, 509, 510, and 511 in turn. At each of these tracks the servo information is read, and an offset number is stored. These offsets ,called phase 0 through phase 3 offsets, represent the non-linearity of the scale over four tracks (scale line to scale line) and are used to compensate for this non-linearity.

The heads are then stepped outward, 64 tracks at a time, to the beginning track of each of the eight thermal zones. At each track the servo data is again read and the difference between this reading and the phase 0 offset is computed and stored as the zone's thermal offset. At the same time the zone timer for this zone is reset. The timers are automatically updated by the processor every index. This re-zero operation takes approximately 3 seconds to complete, and occurs any time power is applied. The sequence may be commanded from the controller at any time by driving pin 6 on the control cable with jumper C installed. Once the re-zero operation has completed properly the processor activates the SEEK COMPLETE line. From now on, as long as the heads are positioned on a track, each time the index pulse is detected the servo data will be read, the thermal offset for this zone will be updated its zone timer reset and the other zone timers updated. In this way the current zone thermal offset is continuously updated. The drive is now ready to be selected by the controller.

When DRIVE SELECT "X" is driven true and matches the drive select jumper, the drive select logic enables the interface logic to gate control and data signals to and from the drive. The drive will read or write data on the selected head at the present track depending on the state of the WRITE GATE line. The read/write circuits transfer the MFM data as required.

The drive may be commanded to move the heads by receiving step pulses. The pulses can be sent in one of two modes:

1) Normal mode, in which the step pulses are sent slower than every 1.5 msec.

2) Buffered mode, in which the step pulses are sent faster than every 600 usec.

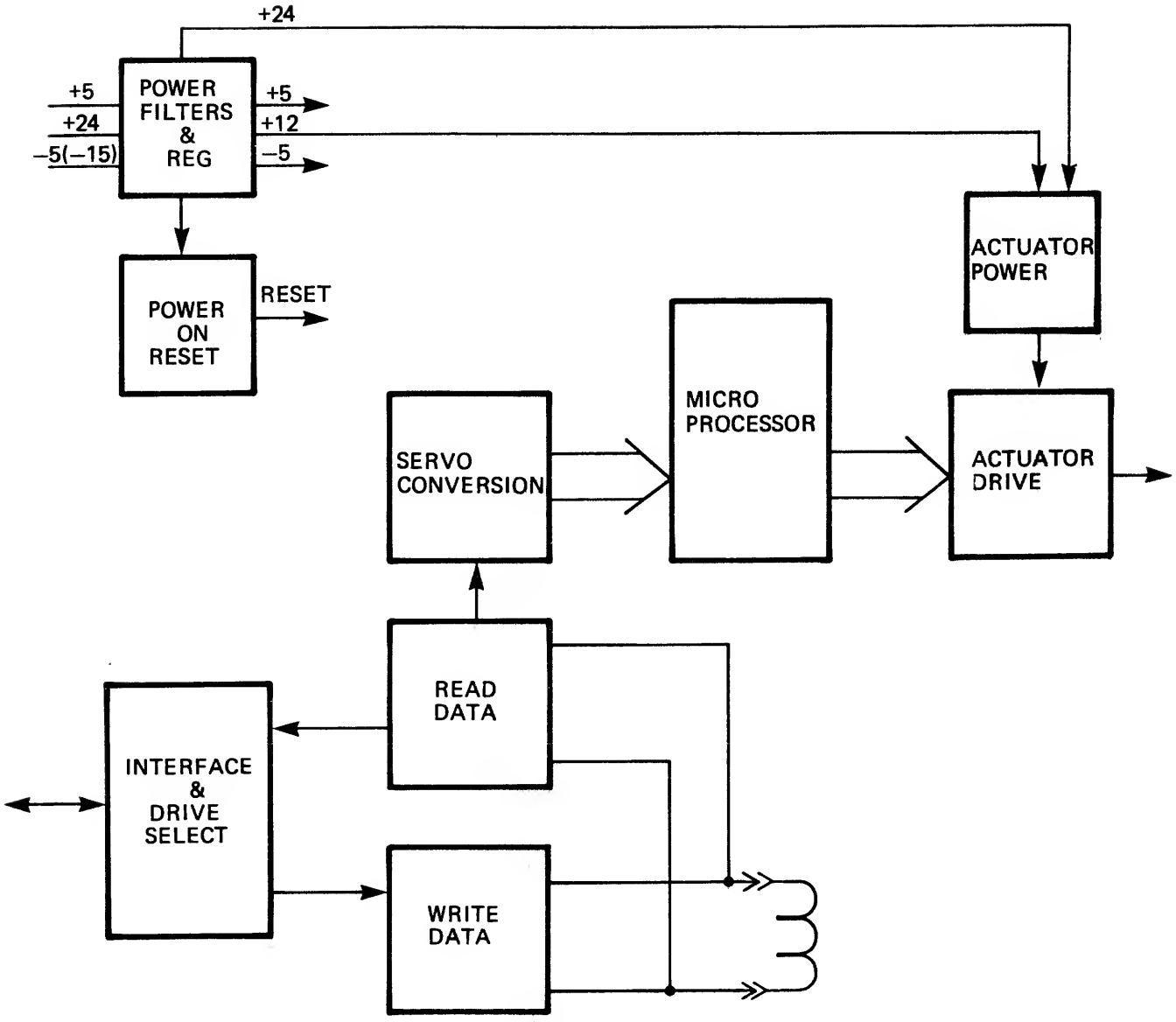


FIGURE 4-8
DRIVE CONTROL PCBA BLOCK DIAGRAM

Step pulse rates between 600 usec and 1.5 ms cause unpredictable results and are not allowed. If the steps are received in normal mode, SEEK COMPLETE is driven false and the processor commands the actuator drive circuitry to start the heads moving in the direction specified by the DIRECTION IN line immediately on receipt of the step pulse. If step pulses are received in burst mode, SEEK COMPLETE is driven false and the processor waits until all steps have been received before commanding the move. In either case, the encoder signals are used to monitor track crossings and indicate when the heads are on track. Once the heads have reached the target track the processor applies the phase offset and checks the zone timer. If the timer indicates less than five minutes the thermal offset for this zone is applied and after a suitable delay to allow the heads to settle on-track SEEK COMPLETE is driven true. If, however, the zone timer indicates that more than five minutes have elasped since this zone offset was last updated, the processor waits for index, reads the servo data, resets the timer and updates the thermal offset. This updated zone offset is then applied, and after settling, SEEK COMPLETE is driven true. The following paragraphs describe the operation of the drive control board in greater detail.

4.3.3.2 D.C. Power Filter and Regulators

Refer to Figure 6-2 location C6 and 7. The three required DC voltages connect to the drive via connector J5. +24 VDC enters on pin 1 where L15, C93 and C89 form a decoupling network. Voltage regulator VR1 uses +24 VDC as an input and outputs +12 VDC used by some of the operational amplifiers in the drive. The +24 VDC is used by both the write current drivers and the actuator drivers. The +24 VDC return line is J5 pin 2.

+5 VDC enters on pin 5 and is decoupled by L16, C80 and C79 before being supplied to the logic on the PCBA. +5 VDC is further filtered by L11, C35 and C97 to be used by the read channel amplifiers as +5 V*. The +5 VDC return line is J5 pin 6.

The minus voltage supplied to the drive may be either -5 VDC or -7 VDC to -16 VDC and enters at J5 pin 4, where it is decoupled by L14, C94 and C95. If the minus voltage is more negative than -5 VDC then regulator VR2 regulates the input voltage to -5 VDC. The regulator output is selected by placing the jumper in the -15 VDC position (all drives are shipped from Quantum with the jumper in the -15 VDC position).

> CAUTION: Damage to the drive can occur if minus voltages greater than -5 VDC are applied to the drive when the jumper is in the -5 VDC position.

The -5 VDC is further filtered by C87, L6 and C98 to be used by the read channel as -5 V*. The minus voltage return line is J5 pin 5.

4.3.3.3 Power On Reset

The purpose of the power on reset circuitry is two-fold. First the reset will hold the processor and other circuits in a known condition (reset) until the logic power is up and stable. Secondly, it provides a reset when the logic power falls below an acceptable level. The circuitry is located at C5 and 6 on Figure 6-2. As the +5V rises, C46 charges via R73. Once this charge exceeds the high level input voltage of OR gate 7H (nominally 1.4V) the gate outputs a LO at pin 10. This is -POR and is distributed throughout the PCBA to reset the logic.

Transistor Q6 is held cutoff until diode CR13 conducts. This will not occur until the +5V exceeds +3V for approximately 10 msec as determined by resistor R75 and capicator C47. At this time Q6 will conduct, discharging C46 causing 7H-10 to go HI. The signal -POR can also be generated by driving the RE-ZERO line LO when the drive is selected and jumper 'C' is installed, this causes 7H-8 to go HI resulting in the -POR signal at 7H-10.

4.3.3.4 Interface and Drive Select Logic

This logic preforms three functions in Series 2000:

1) Provides cable drivers and receivers for the interface signals.

2) Allows for gating these signals with the DRIVE SELECT line.

3) Provides for interface cable termination on the last drive on the cable.

Refer to Figure 6-2 , page 6-3 of this manual. At the top of this figure (5, 6 and 7D) are the cable receivers for the REDUCED WRITE CURRENT, HEAD SELECT, DIRECTION IN, STEP, and WRITE GATE control signals. The REDUCED WRITE CURRENT line is received by buffer 5C, a 7407, at pin 9. The other signals are received by the hex Schmitt trigger inverter, a 7414, at 7J. All of these signals may be terminated at this drive by installing a 220/330 ohm resistor pack at 6J. The RE-ZERO line may be enabled by placing a jumper across point C.

At page location 7C is the DRIVE SELECT jumper block and the DRIVE SELECT terminator R90, R100. Placing a jumper across point A results in the drive being continuously selected and is normally used for test purposes. When a LO signal on a DRIVE SELECT line matches with a jumper, gate 7H is enabled to receive the optional RE-ZERO command. +DR SEL (2F-8) will enable reception of STEP (4J-11) and WRITE GATE (4J-8). +DR SEL also provides the -DRIVE SELECTED signal via 2F-6 over the data cable (J2-1) to indicate to the controller that the drive has been selected. The signal +DR SEL also enables the differential line driver 2J at 3C to output $\pm$ MFM RD DATA to the controller. The WRITE FAULT F/F 6H at 3D is also enabled to latch a fault condition in the event write current is detected (6H-3) and there is no WRITE GATE present (6H-2). If this error is detected and latched it is necessary to raise the DRIVE SELECT line to reset the error (5H-5). +DR SEL also goes to Figure 6-3 at location D8 where at location 3D it enables the -TR000, -RDY, and -SK COMPLETE control signals at gate 5J. At location 7B OR gate 3F-5 will disable the head select decoder 5A by selecting an output greater than seven if +DR SEL is LO. The signal +DR SEL is also an input at location 3D on Figure 6-4 , where it enables the -INDEX control signal at gate 2F.

4.3.3.5 Write Data Circuits

Figure 4-9 is a functional block diagram of the write circuits found in the Series 2000. The write enable circuit insures that the +5 V logic voltage is present, the drive is selected, on track, READY, it is not index time (to prevent writing in the servo area), and WRITE GATE is active. When these conditions are met the write enable switch turns on the write current source.

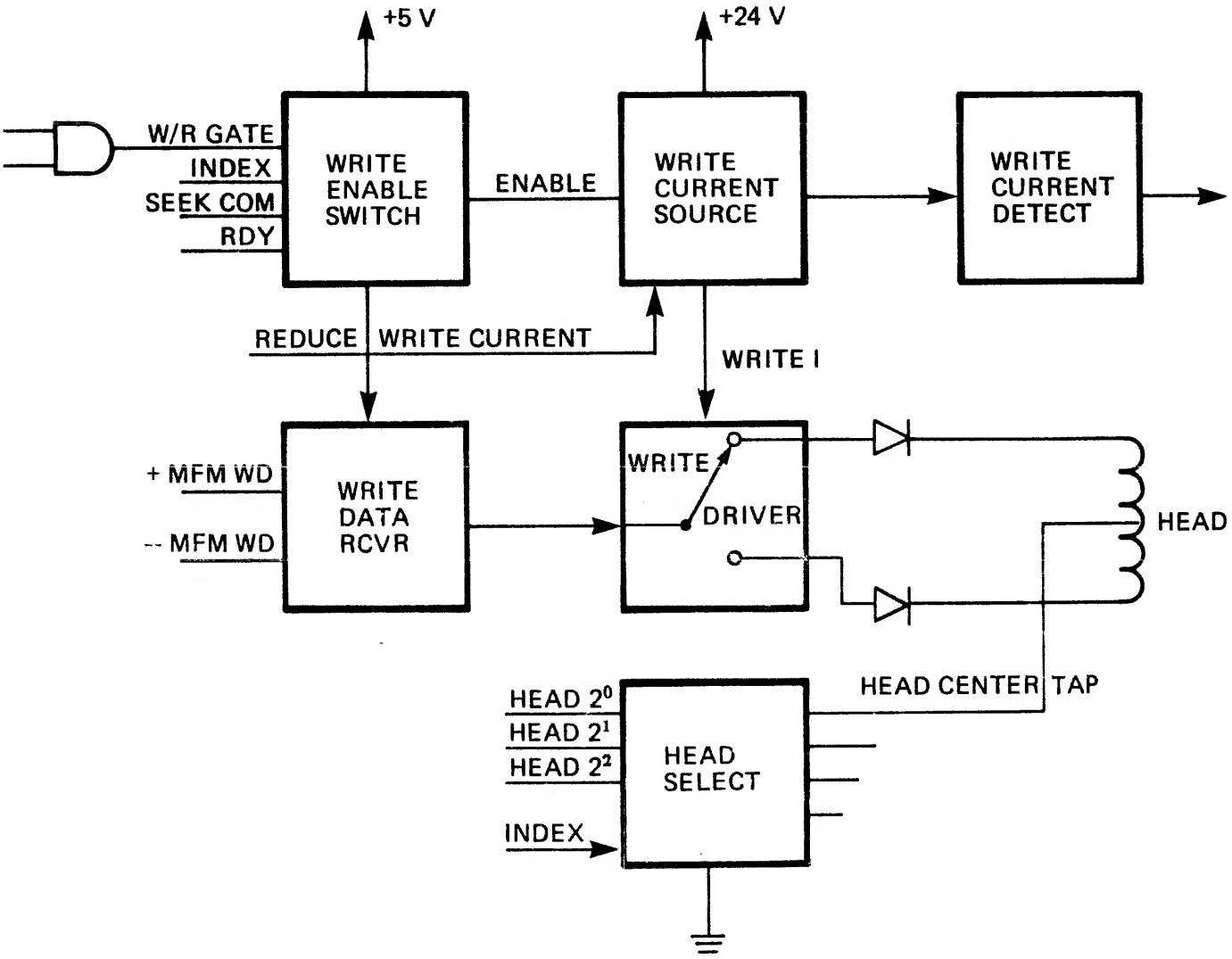


FIGURE 4-9
WRITE CKT BLOCK DIAGRAM

This constant current source provides the write driver with 75 ma of write current or 65 ma when the REDUCED WRITE CURRENT line is true (LO). Reduced write current is used on the inner tracks to help reduce pulse crowding a cause of bit shift. The circuit also provides a current on signal which is used by the write current detector to set the write fault flip flop. The write driver receives its switching input from the write data receiver and will switch the write current into one end or the other end of the head coil whose center tap has been grounded by the head select switch. The head select switch will ground the selected head center tap except during index time when head 0 is always selected so that the servo information may be read.

Figure 4-10 is a simplified schematic of the write enable switch found on Figure 6-3 , location A and B, 5 through 8. The logic to generate +WRITE is found on Figure 6-2 , location A and B, 1 through 8. Transistor Q4 is the current enable switch that will turn on when current flows through R67, causing A4's base to be less positive than its emitter. In order for current to flow in R67 transistor Q5 must conduct. Q5 will conduct when the +5V is greater than 3.5V due to the action of R71, the base emitter junction of Q5, and CR14 a 3.0 V zener diode, and the +WRITE signal is true. The +WRITE signal will only be true if all of the following conditions are met:

1) The drive is selected (4J-10 HI)

2) WRITE GATE is true (4J-9 HI)

3) The drive is READY (4J-2 HI)

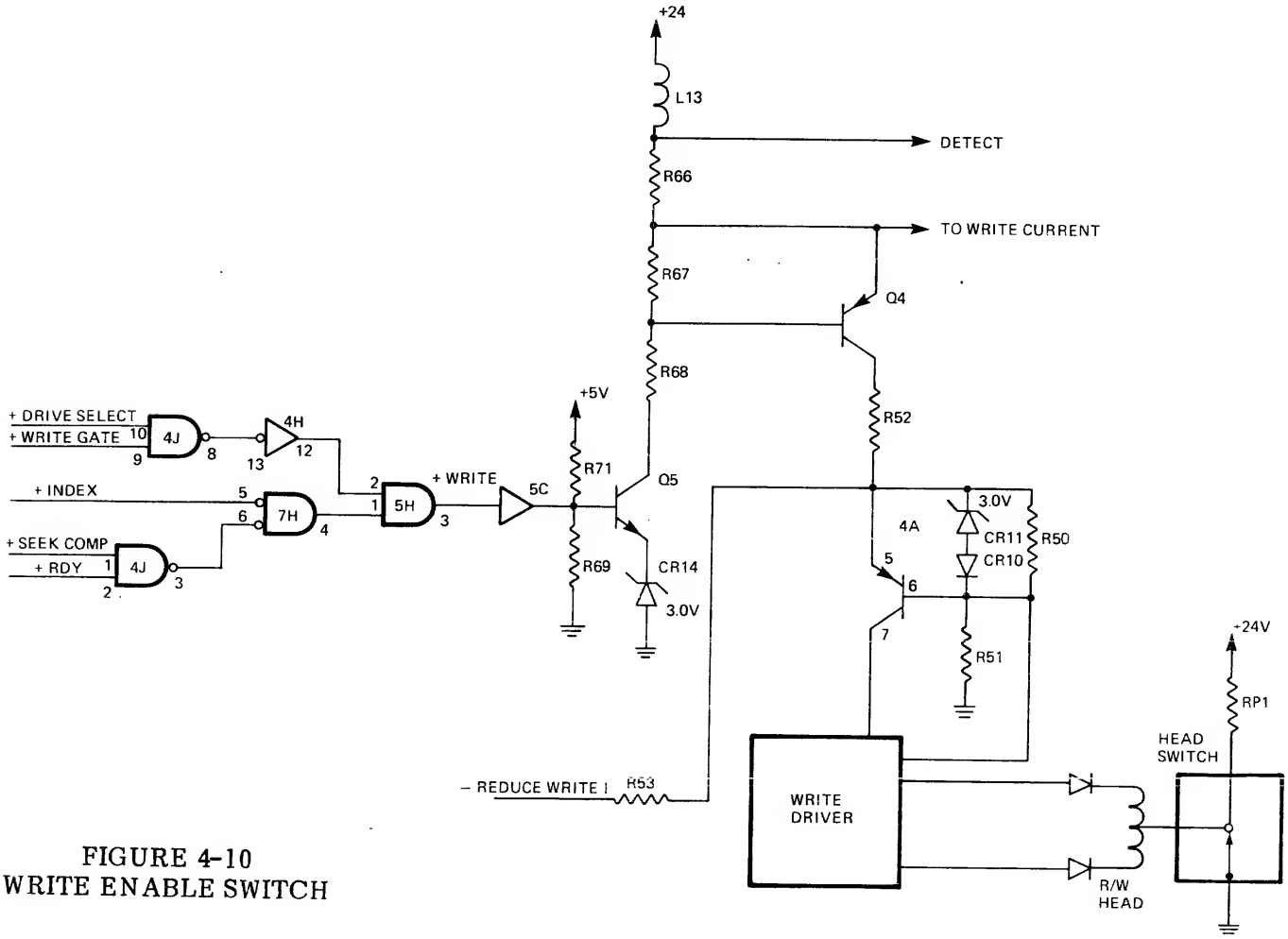


FIGURE 4-10
WRITE ENABLE SWITCH

4) The drive is on track (4J-1 HI)

5) Index is not true (7H-5 LO)

When these conditions are met current is supplied to the constant current source 4A via the current resistor R52. Diodes CR10 and CR11 set a reference voltage across R52 and 4A to maintain a constant current flow through 4A during voltage flucuations of the +24 V supply. Resistors R50 and R51 provide a current path for the write driver to shut off when Q4 is turned off. The write driver switches the write current between the windings of the selected head.

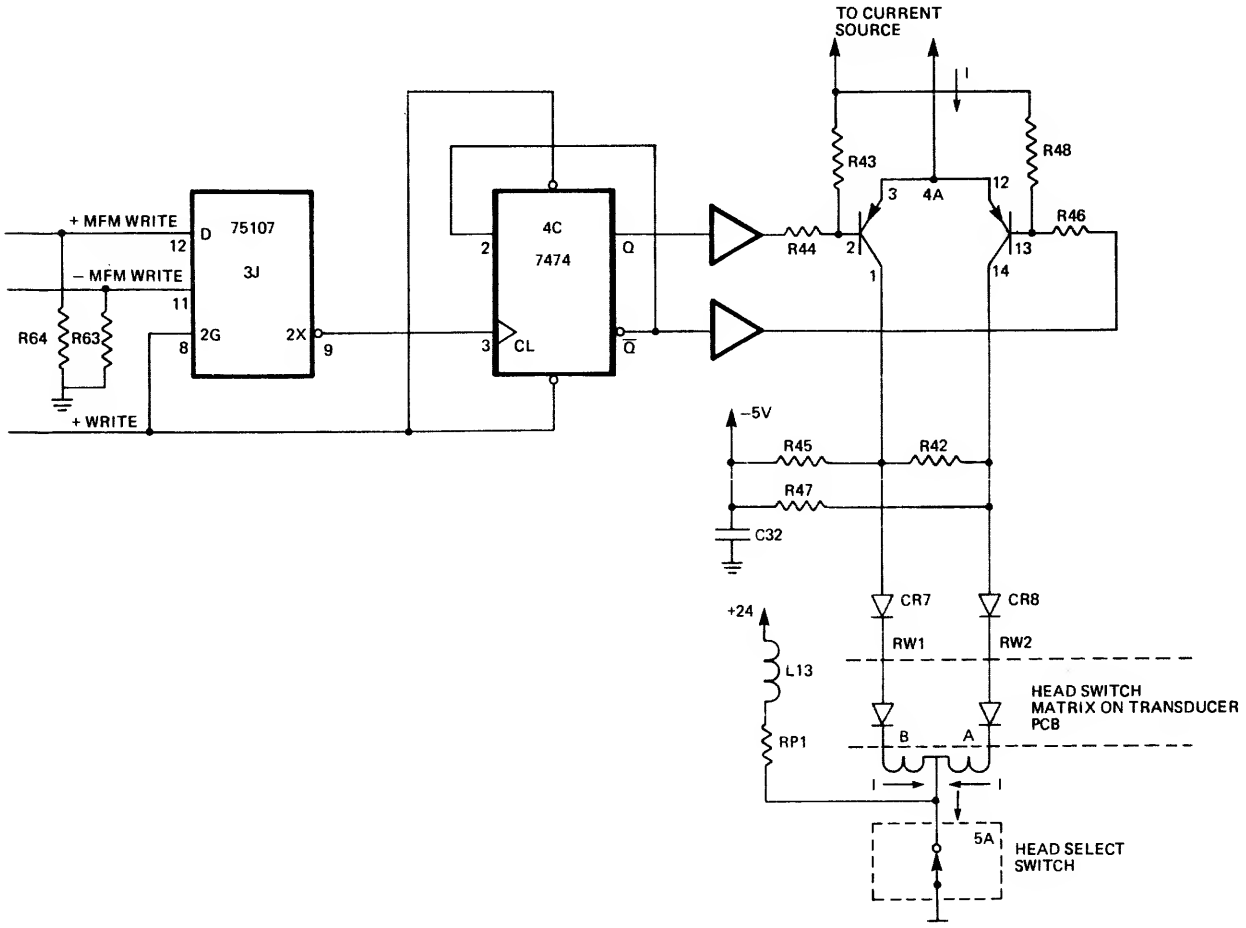


FIGURE 4-11
WRITE DATA RECIEVER AND SWITCH

Figure 4-11 illustrates the operation of the write data receiver found on Figure 6-2, B7 and the write driver found on Figure 6-3, A6. When +WRITE enables the differential line receiver 3J, a 75107, the differential MFM WRITE DATA signal terminated by R64 and R65 is converted to a TTL signal at output pin 9. When the +MFM WRITE DATA signal goes more positive than -MFM WRITE DATA signal the TTL output will switch HI. Since +WRITE removes the preset and clear inputs from the write data flip flop 4C the flip flop will toggle to the opposite state. If we say the Q output (4C-9) switches LO, then 4A-13 goes LO and this side of the driver turns on.

Current will flow from the constant current source through the transistor, through CR8, through the head switch diode, through coil A of the head and to ground through the head select switch 5A. When the next pulse arrives (4C-3) the F/F switches states, 4A (1,2,3) conducts, and current flows through head coil B. Resistor R42 is used to prevent oscillations in the head coil by providing a damping path. Resistors R45 and R47 will cause diodes CR7 and CR8 to be reverse biased when the write current is shut off. Inductor L13 and resistor pack RP1 cause the head switching diodes of the unselected heads to be reverse biased.

The head select switch 5A is a one of ten decoder. The three low order input bits are the +HEAD 2^0, 2^1 and 2^2 signals, and its high order bit will only be LO if the drive is READY and index is not present. Based on the binary configuration of the +HEAD bits and the output of 3F-6 only one of the outputs will be LO. This LO provides the ground path for current through the selected head. Inverter 5B, pins 1 and 2 force the selection of head 0 during index to allow reading of the servo data from surface 0.

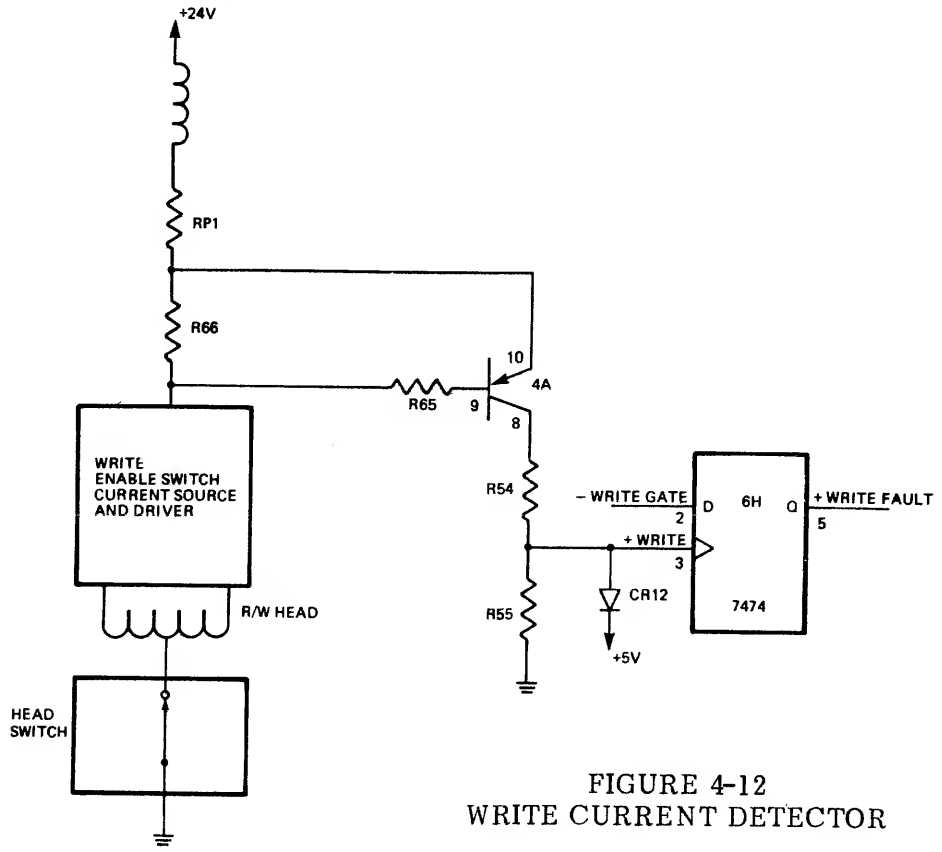


FIGURE 4-12
WRITE CURRENT DETECTOR

Figure 4-12 illustrates the write current detector used to trigger the write fault flip-flop 6H. The flip-flop is at 4D on Figure 6-2. The remainder of the circuit is found on Figure 6-3 at B6. Transistor 4A (8, 9, and 10) remains in the off state until current flows though R66. The positive to negative drop across R66 causes 4A to turn on allowing current to flow through R54 and R55 to ground. The positive voltage drop across R55 is clamped to +5 V and will clock the write fault flip-flop 6H set if the WRITE GATE signal is not true (HI) and the drive is selected.

4.3.3.6 Read Data Circuits

The block diagram shown in Figure 4-13 illustrates the functional areas of the Series 2000 read channel. When the head select switch connects the center tap of the selected head to ground, the diodes in the head coupling network are forward biased. As magnetic flux changes pass by the head coil current is induced into the coil. This current is coupled through the head coupling diodes and appears as small differential voltage changes at the input of the pre-amplifier. The pre-amplifier amplifies these changes which are then passed through a low pass filter to eliminate unwanted high frequency noise. The signal is again amplified and filtered before being input to the differentiator which converts the voltage peaks of the signal to zero voltage crossings. These zero voltage crossings, representing the flux changes read from the disk, are input to a comparator which converts the sinesoidal signal to a square wave to drive a pulse generator. This pulse generator is enabled whenever the drive is not writing and will output a pulse each time its input switches. The pulse train is filtered by a droop ignore circuit and is input to a differential line driver. The output of the line driver is the ± MFM READ DATA sent to the controller via the 20 conductor data cable.

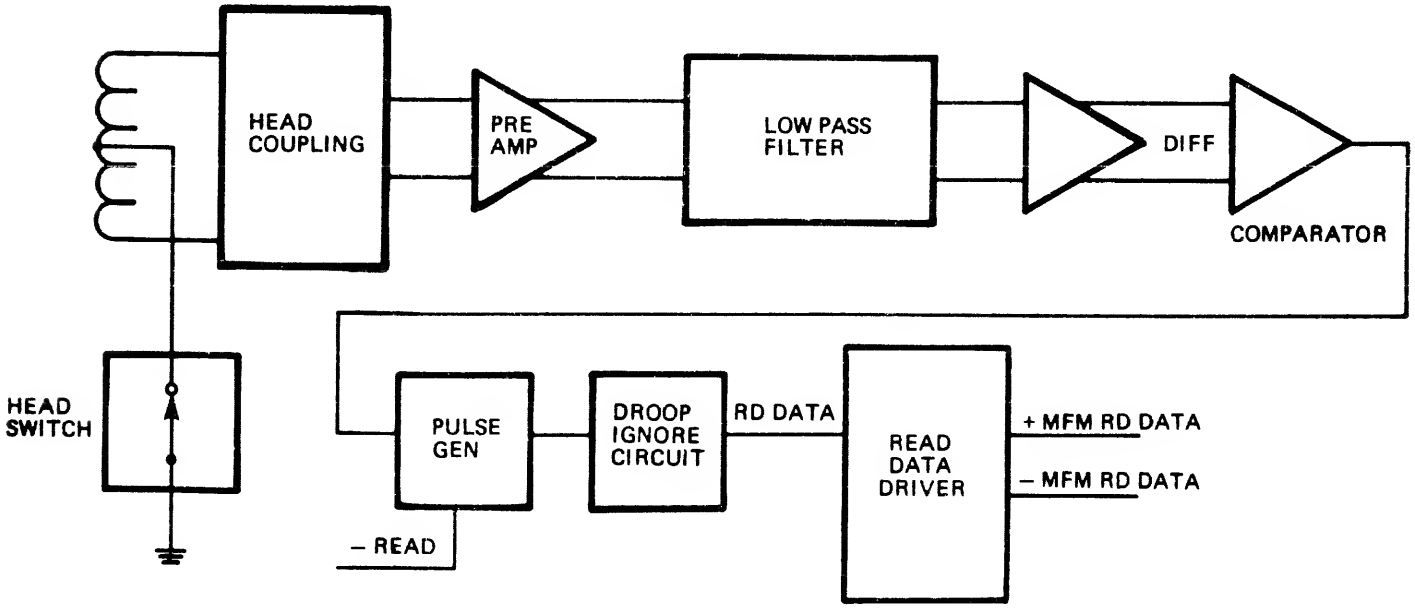


FIGURE 4-13
READ CHANNEL BLOCK DIAGRAM

The function of the droop ignore cicrcuit is to eliminate false data pulses from the pulse train. These pulses may be generated when the differentiated signal droops toward zero volts when reading low frequency data patterns and noise causes the signal to cross zero between legitimate bits. Figure 4-14 illustrates the effect and the function of the droop ignore circuit.

Signal 1 shows an amplified 1F pattern, after filtering and differentiating the signal will look similar to 2. Where signal 1 had a slow rate of change (between flux changes) the differentiated signal droops toward zero volts. The output of the comparator should be as shown by the solid line in signal 3. Noise in the read channel could cause the droops in signal 2 to cross zero volts giving the extra pulses shown by the dashed lines in 3. The result would be extra bits in the output signal 4. Adding a one-shot and the flip/flop (droop ignore) between the comparator and the pulse generator prevents the extra pulses from triggerring the pulse generator. Signal 5 is now the pulse generator input and the resulting output is signal 6 with no extra bits.

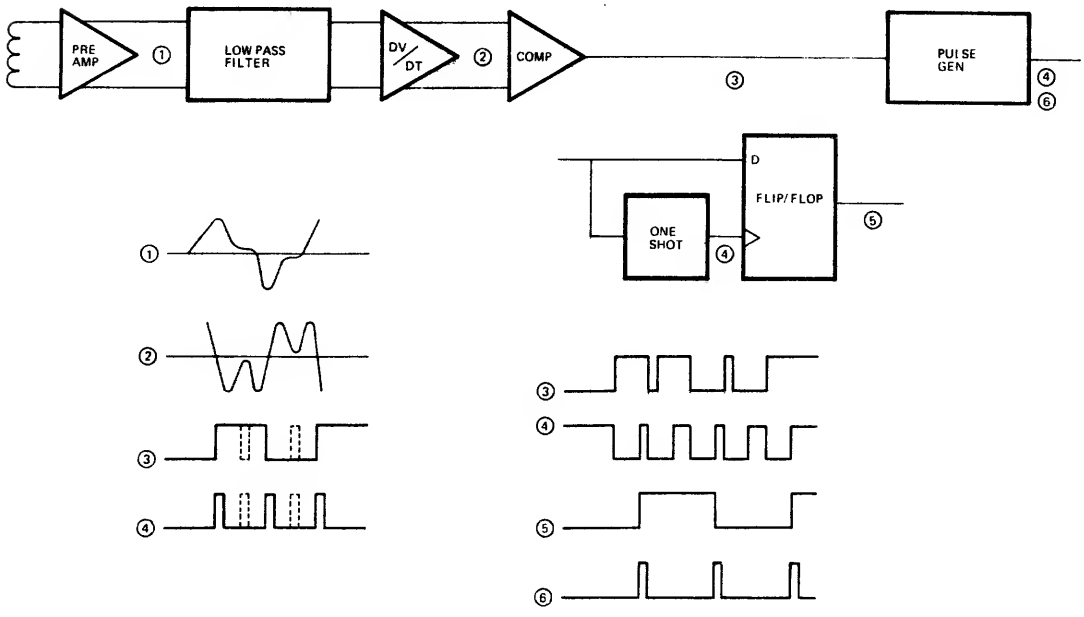


FIGURE 4-14
READ DROOP AND DROOP IGNORE

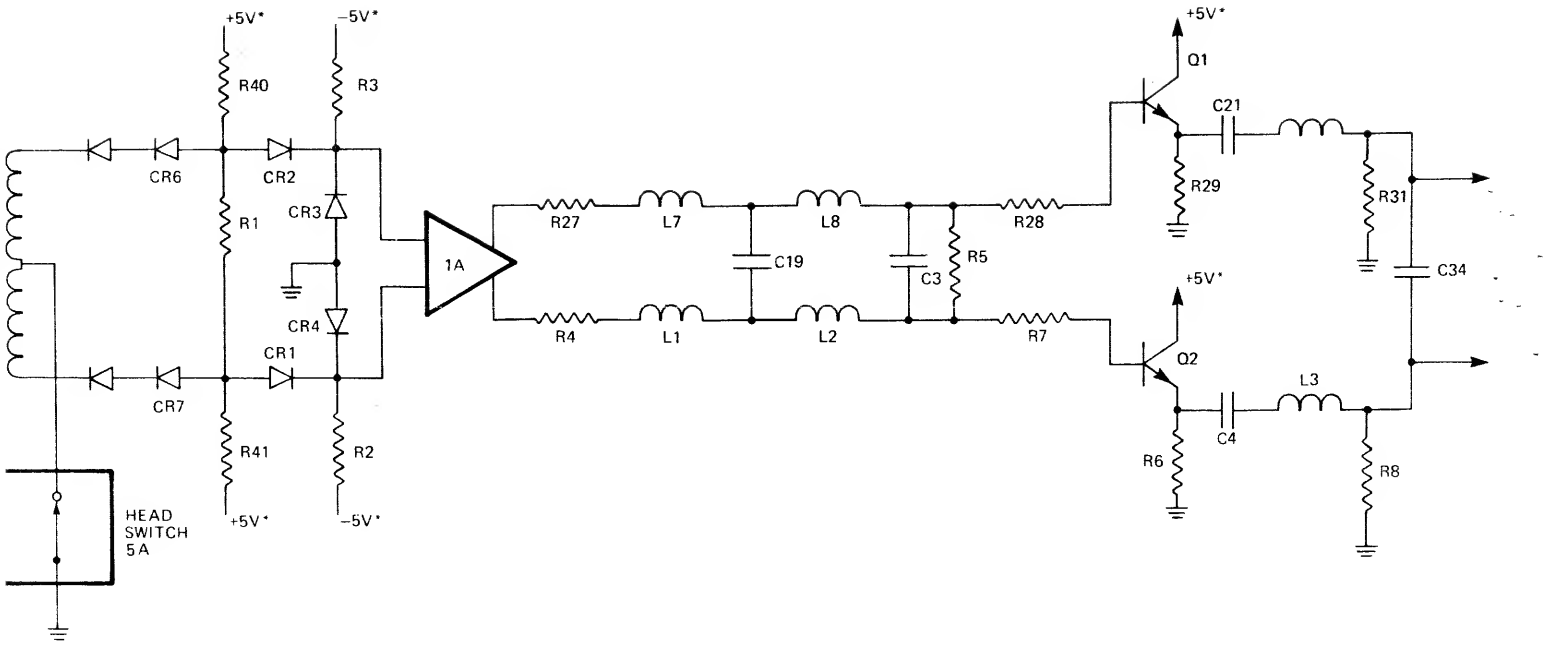


FIGURE 4-15
READ CHANNEL FRONT END

Figure 4-15 is a simplified schematic of the actual read channel, up to the differentiator input, that appears on Figure 6-3 at C1 through 5. Diodes CR1, CR2, CR6, and CR7 and the head select diodes found on the transducer PCBA form a diode switch that is forward biased when write current is removed from the head. In the static state, that is no signal present in the head coil, about 1.4 ma of current flows through the diodes and each side of the head coil, the current flowing in both head coils causes the flux to be cancelled and it has no effect on the media. If, however, there are flux transisitions passing under the head, the induced current will modulate the 1.4 ma bias current and provide a voltage input to pre-amplifier 1A. Diodes CR3 and CR4 protect the amplifier input during write operations. Resistors R40, R41, R2 and R3 provide the bias current for the head coupling bridge while resistor R1 is a damping resistor used to prevent oscillations in the head coil. The gain of the pre-amplifier is about 400 and the amplified differential output is applied to a low pass filter. The read signals are processed in a differential mode up to the comparator to reduce common mode noise. The low pass filter is comprised of R27, R4, L7, L1, C19, L8, L2, C3, R5, R28 and R7. The filtered signal is coupled to another filter by emitter followers Q1 and Q2.

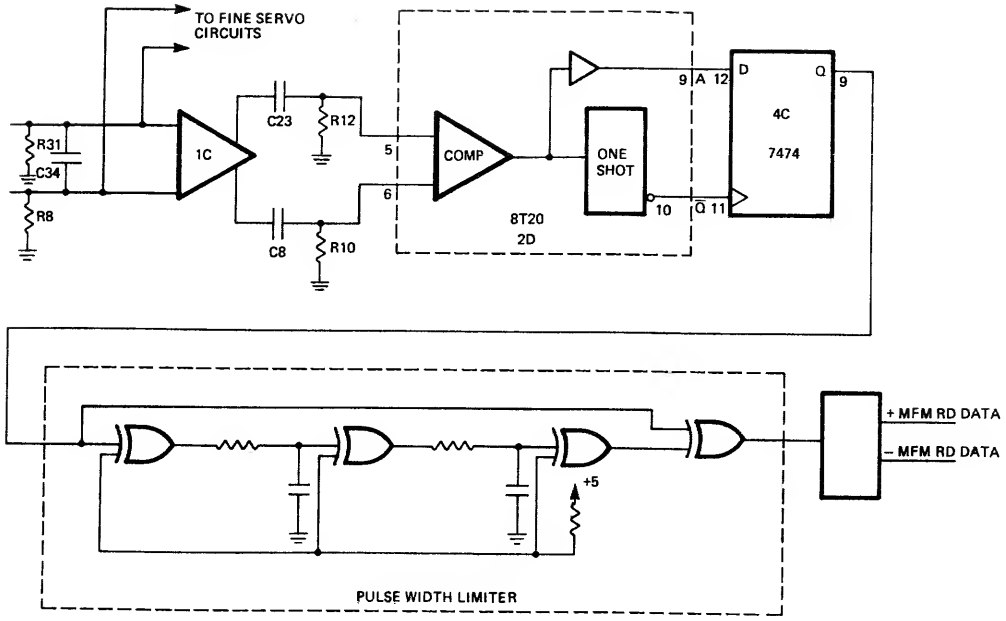


FIGURE 4-16
REMAINDER OF READ CHANNEL

Up to this point flux changes on the media that have been detected, amplified, and filtered are in the form of voltage peaks. Since the precise bit timing required by the data separator is not easily achievable by peak detection; the data is differentiated to accurately convert the peaks into zero voltage crossings. Figure 4-16 illustrates the remainder of the read channel. Amplifier 1C is configured as a differentiator with the differentiated outputs appearing at the input to the comparator. The zero crossing are detected by the comparator, whose output is the D input of flip-flop 4C part of the droop ignore circuit. The zero crossings also trigger a one shot whose period is set shorter than the expected bit time. When the one-shot times out the flip-flop latches the state of the comparator. The one-shot time is long enough that any change in the comparator output due to noise in the differentiated signal will be filtered by the flip-flop and not be detected as data bits. The output of the droop ignore flip-flop is then passed through a pulse width limiter comprised of a series of gates with added delays. The resulting narrow positive pulses represent the detection of flux reversals in the media. These pulses are input to a differential line driver and are output as $\pm$ MFM READ DATA to the controller via the 20 conductor data cable.

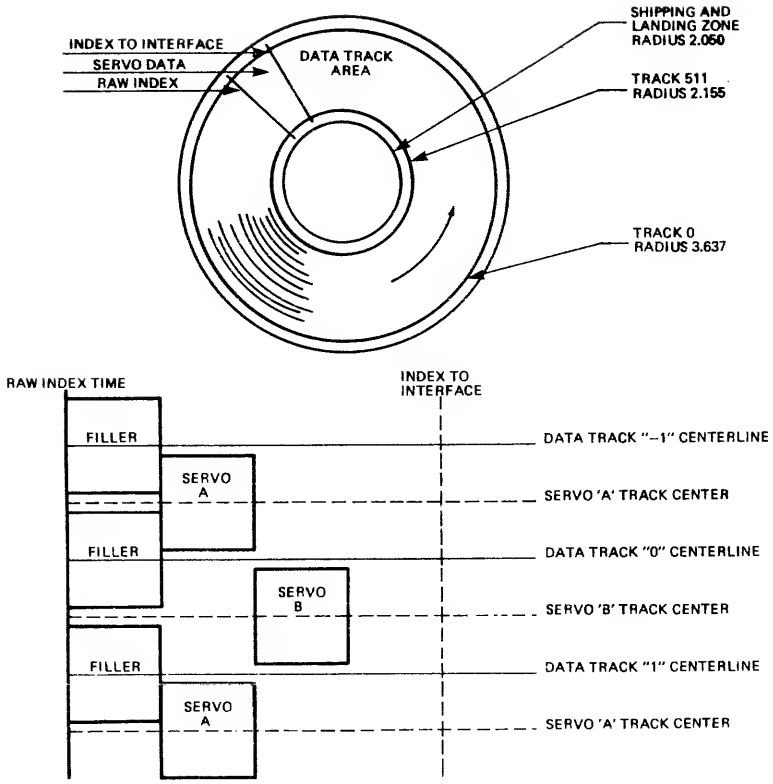


FIGURE 4-17
SERVO DATA POSITION

4.3.3.7 Servo Read and Conversion Circuits

The Series 2000 uses an "embedded" servo burst to compensate for thermal changes within the drive. This servo burst is recorded at the beginning of each track on surface zero (the lowest surface). The burst period is approximately 600 usec long and occurs immediately after 'raw' index (the actual physical index). The burst is composed of: a 1F filler pattern written on data track center followed by two 1F servo patterns written one-half track either side of the data track center. Index is reported to the interface after these bursts have passed.

To maintain track timing compatibility with competitive drives the Series 2000 disk rotational speed is slowed by about 4% which allows 19.2 ms for user data. Figure 4-17 illustrates the position of the servo burst on disk surface 0 and its position between tracks.

The servo read and conversion circuits are used to detect the servo bursts and convert this analog information to digital values which are then used by the processor to locate the heads on the actual track center, as the track center indicated by the optical scale may be incorrect due to thermal changes in the drive. A functional block diagram of the circuits associated with this servo system is found on Figure 4-18. The actual circuitry is found on Figure 6-4 , page 6-5 , location C and D2 through 8. Refering to the block diagram, the operation is as follows: The amplified and filtered read signal is seperated from the normal read channel prior to the differentiator and input to an amplifier. This amplifier provides the additional gain required by the peak detector. (In the servo circuitry we are interested in the amplitude of the single frequency burst and not the timing of individual flux changes, therefore there is no need to use the differentiator found in the normal read channel.) The peak detector is turned on by a gate pulse developed by the time slot generator.

The time slot generator starts with raw index and, using clock pulses provided by the processor, counts out the peak detector gate time slot followed by two sample pulses, one for each servo burst. When the peak detector has settled at the peak amplitude of the servo burst the first sample pulse occurs.

This sample pulse turns on the sample and hold for servo A. After a short period of time, servo B is input to the peak detector and its peak determined. The time slot generator outputs another sample pulse and the peak is sampled and held by the servo B sample and hold.

The processor then gates the output of the A sample and hold to the A to D converter and issues the start conversion pulse. When the sample has been converted to a digital value, the processor inputs the digital data and saves it. The process is then repeated for the B sample. Since the A and B servo bursts are recorded one on each side of the data track, the processor can determine from an amplitude comparison the distance and direction the head must move to be centered on the data track.

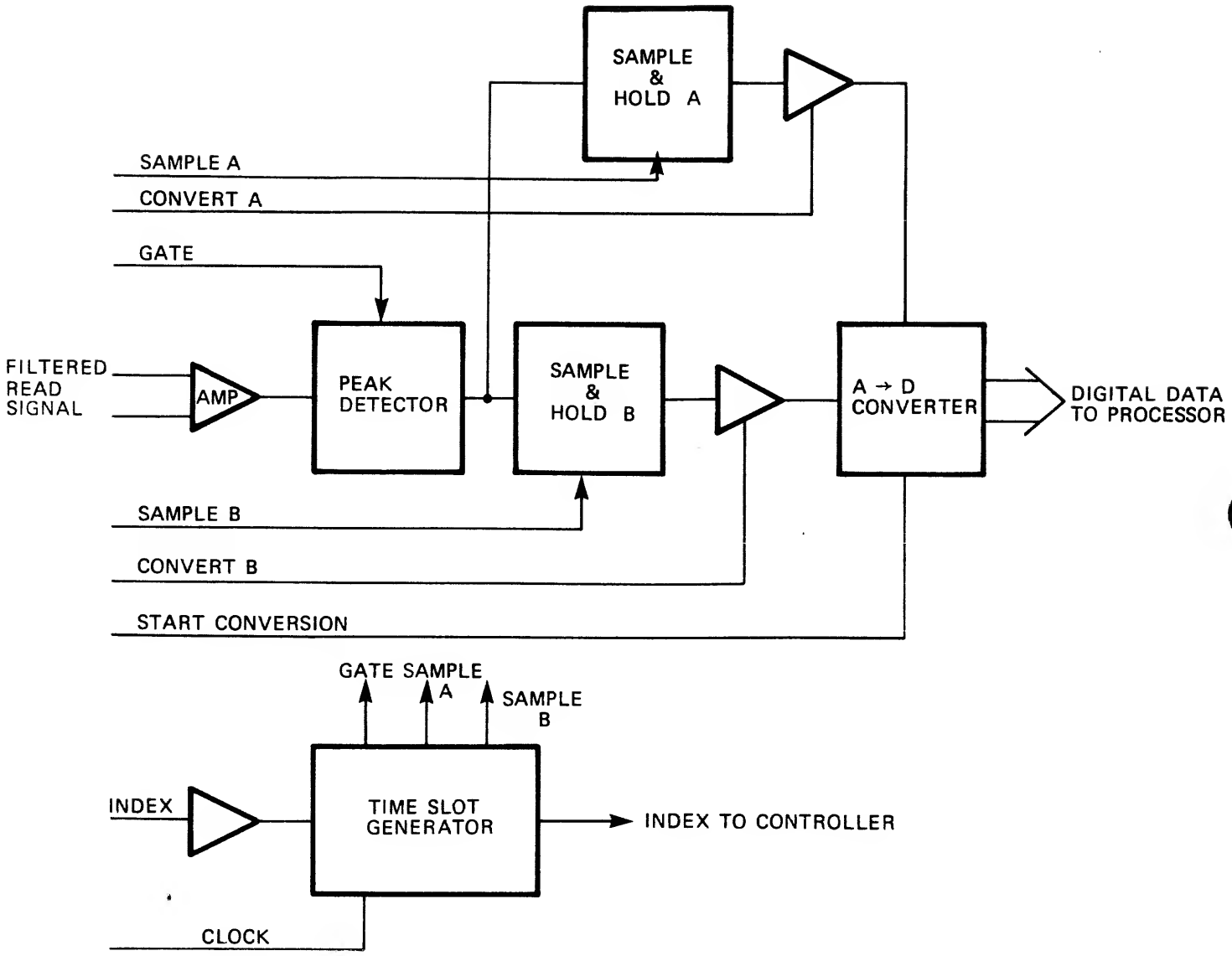


FIGURE 4-18
SERVO CIRCUITRY BLOCK DIAGRAM

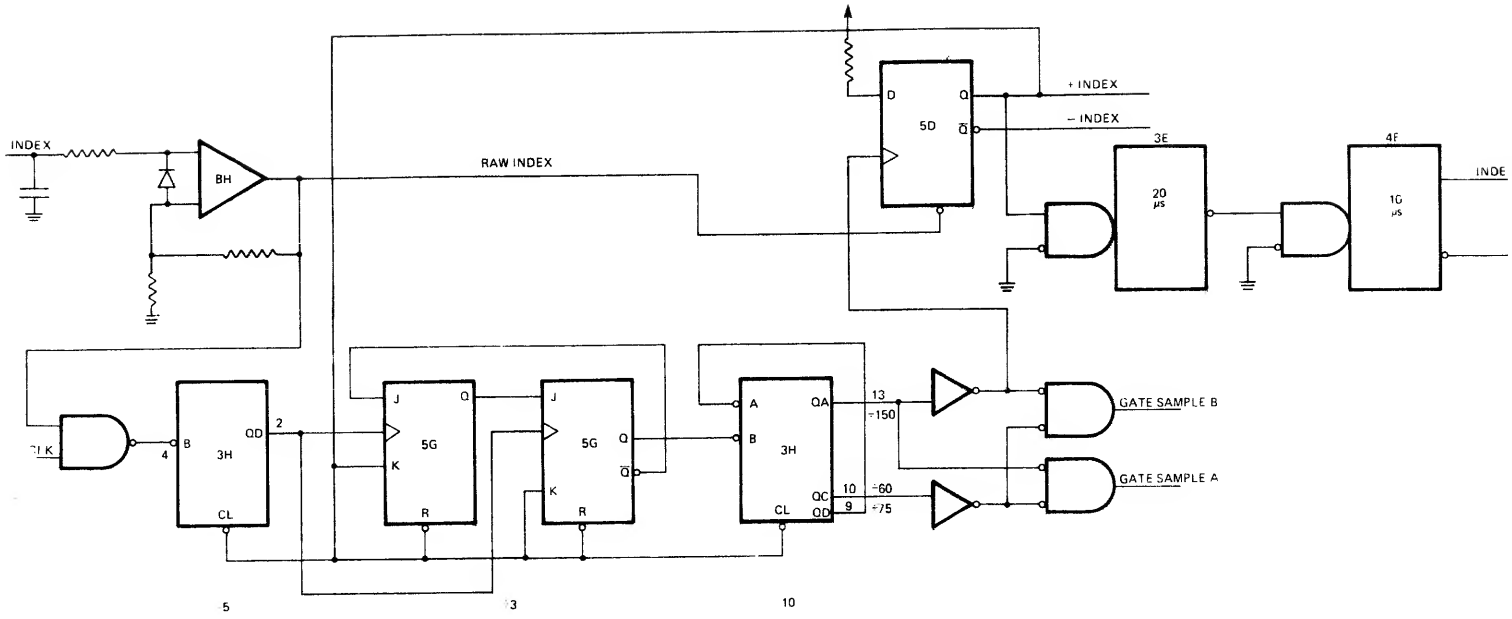


FIGURE 4-19
INDEX AND TIME SLOT GENERATION

Figure 4-19 illustrates the circuits found in the time slot generator. When the pin in the disk mounting hub passes the index pickup a signal is generated. This signal is input to detector amplifier 8H which shapes the signal into a negative pulse which resets the index flip flop 5D and disables gate 4J. This resets the counters, and counter flip flops 3H and 5G and gates the peak detector on. When the pulse returns positive, gate 4J is enabled and the resets are removed. The clock pulses are then divided by the divide by five counter, 3H-7. This output is further divided by the counter flip flops (5G-8 and 3) configured as a divide by three counter. The final counter divides by ten and produces pulses at the divide by four output (3H-10) and the divide by ten output (3H-13). The HI level from the divide by four output and enables the sample A pulse. When the divide by ten output goes HI, the sample B pulse is generated. The sample A pulse is 75 usec long and occurs 300 usec after raw index. The sample B pulse occurs 112.5 usec after sample A. When the sample B pulse ends, the index flip-flop 5D sets. This gates the peak detector off, provides + INDEX to other circuits of the drive, and triggers a 20 usec one-shot 3E. This 20 usec one-shot allows the forced head 0 select to switch off prior to sending INDEX to the interface. When 3E times out it triggers a 10 usec one-shot 4E. The Q output of 4E is the INDEX pulse sent to the interface via cable driver 2F. The Q output of 4E is sent as an interrupt to the processor indicating that the servo data has been sampled and is ready to be converted.

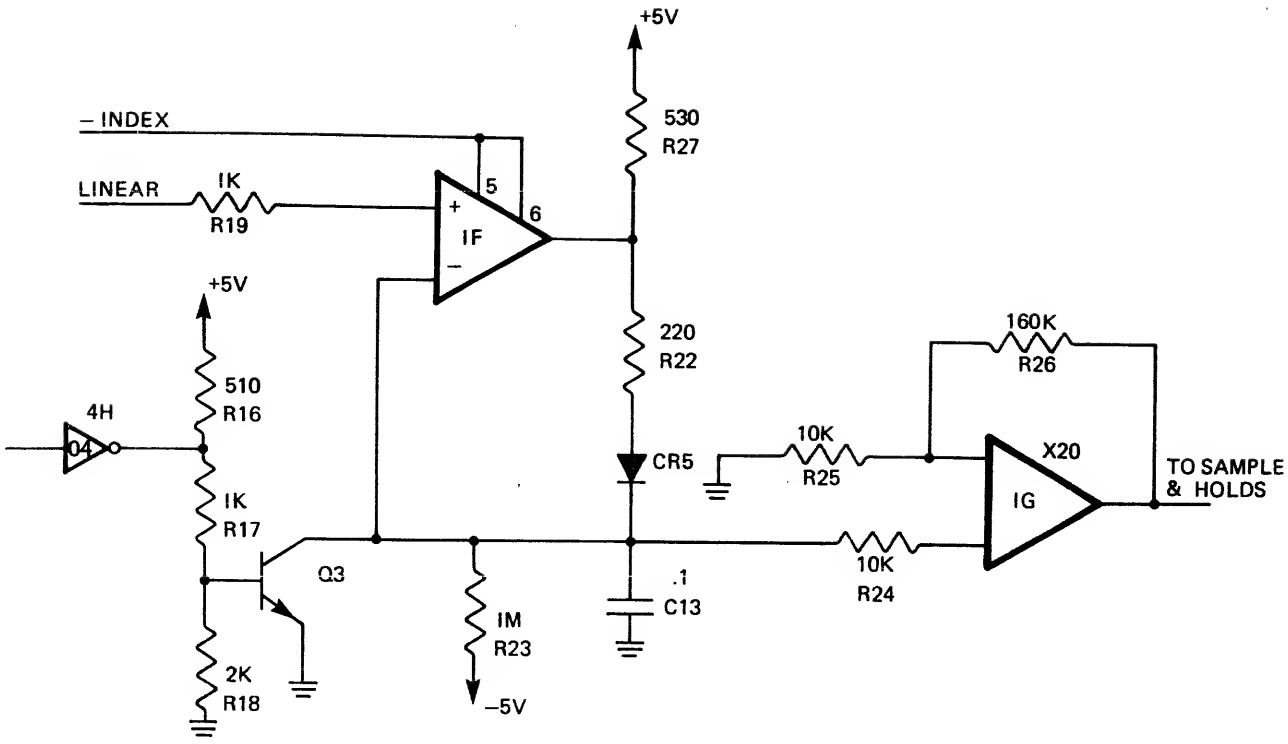


FIGURE 4-20
SERVO PEAK DETECTION

Figure 4-20 illustrates the Servo Peak Detector circuits used in the Series 2000. The input is the filtered read signal which is further amplified by differential amplifier 3C. Peak detector 1F is disabled by the gate signal until the index flip flop (5D-6) is reset. During the time flip flop 5D is set transistor Q3 discharges capacitor C13. When the peak detector is enabled C13 is allowed to charge through R22 and CR5 to a voltage dependent on the amplitude of the pulses output by 1F. The peak value on C13 is amplified by amplifier 1G, with a gain of twenty, then gated to the proper sample and hold by the sample pulse generated by the time slot generator.

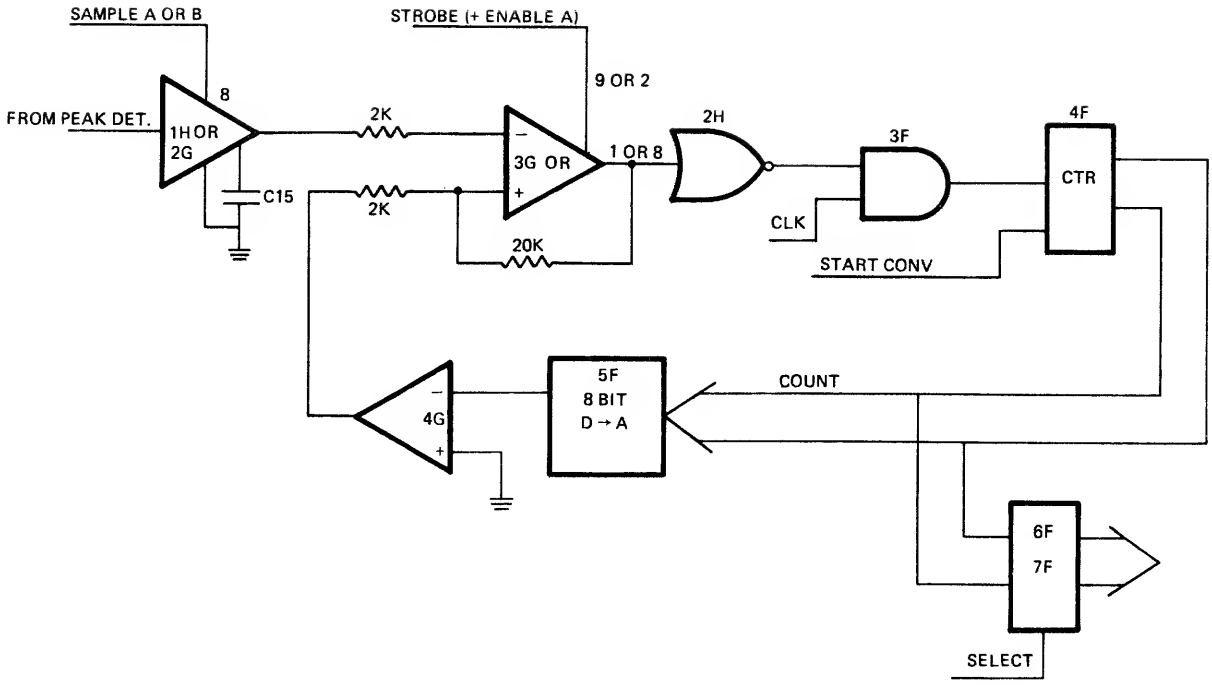


FIGURE 4-21
SERVO A TO D CONVERSION

Figure 4-21 shows the sample and hold and the A to D converter portion of the servo circuits. Only one sample and hold is shown as the circuitry is duplicated for the other sample. When the sample pulse from the time slot generator occurs, sample and hold 1H or 2G samples and holds the output of the peak detector. When the processor is ready to convert this sample it issues the enable signal to comparator 3G and the start conversion signal to reset counter 4F. The counter's digital output is converted to voltage by an eight bit D to A converter 5F and current to voltage converter 4G. Initially, the D to A output is zero and the sample output is some higher value. This difference causes a LO output from the comparator enabling gate 3F to output clock pulses to the counter. Eventually the counter reaches a value that causes the D to A converter's output to match the sample value. When this occurs the comparator outputs a HI to disable gate 3F. The counter now holds a binary number whose value represents the amplitude of the sampled servo burst. The processor will input the digital word via multiplexers 6F and 7F and repeat the process for the servo B data.

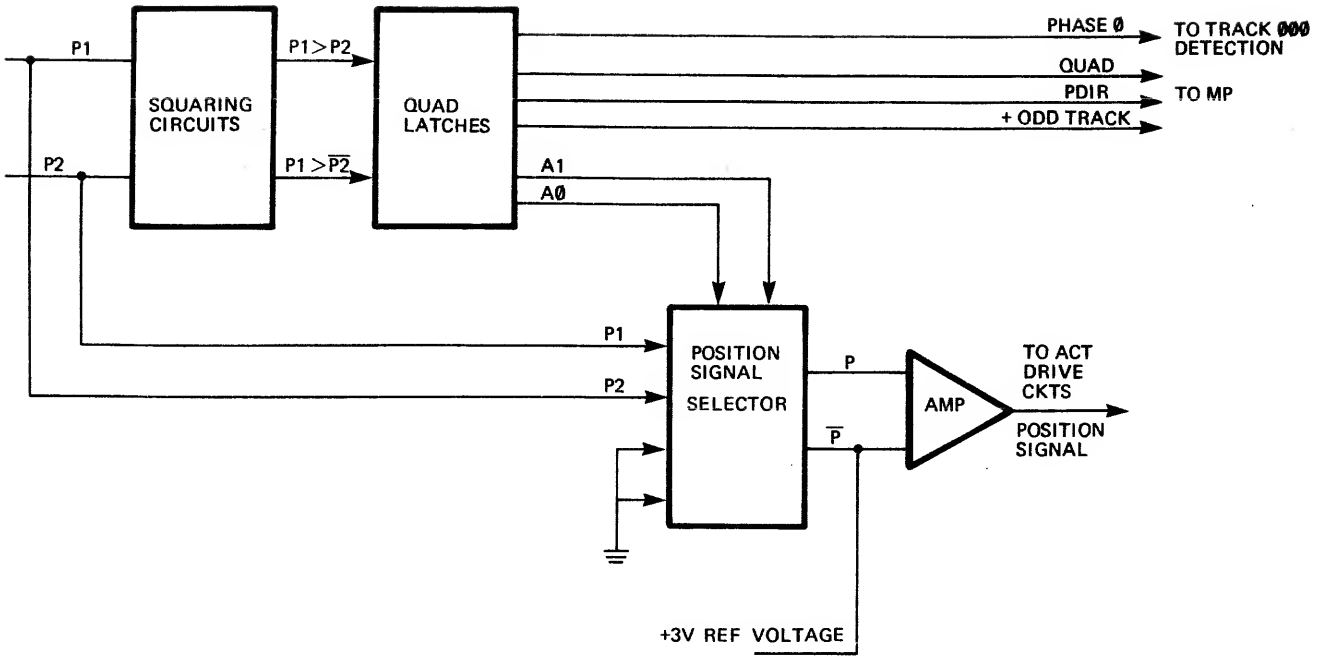


FIGURE 4-22
TRACK POSITION CIRCUITRY BLOCK DIAGRAM

4.3.8 Coarse Position Generation

The block diagram shown on Figure 4-22 illustrates the functional circuits of the coarse track position detector/generator. The circuitry receives the P1 and P2 signals from the transducer PCBA as input. When the scale is moving the signals are two sine waves 90° out of phase. These signals are converted to two square waves 90° out of phase that switch where the linear portion of these sine waves intersect. The square waves are called P1> P2 and P1> $\overline{P2}$ and are applied to the "quad" latches. These latches produce six signals:

- PHASE 0 - used by the track 000 logic to gate TRACK 000 at the correct track.
- QUAD - used by the microprocessor as the track crossing signal.
- PDIR - used by the microprocessor in conjunction with QUAD to determine the actual direction the heads are moving.
- + ODD TRACK - used by the microprocessor to determine the offset voltage polarity.
- A0 and A1 - used as address bits by the analog switch.

The analog switch gates the linear portion of the proper transducer signal to an amplifier that adds a + 3V offset to the signal. (The +3V is the null voltage of the actuator drive circuit.) Summing the analog switch output with this reference produces a 2V peak to peak ramp voltage centered about +3V. The points at which this ramp crosses +3V are the same points where the P1 and P2 signals cross zero volts and are the scale defined track centers. The ramp peaks represent the voltage required to move the heads to a position midway between adjacent track centers. The scale track centers are used by the actuator drive circuits as a reference only. The actual track center is determined by summing the reference voltage and the servo defined thermal offset voltage. This method compensates for both thermal variations within the drive and any non-linearity of the scale and reticle.

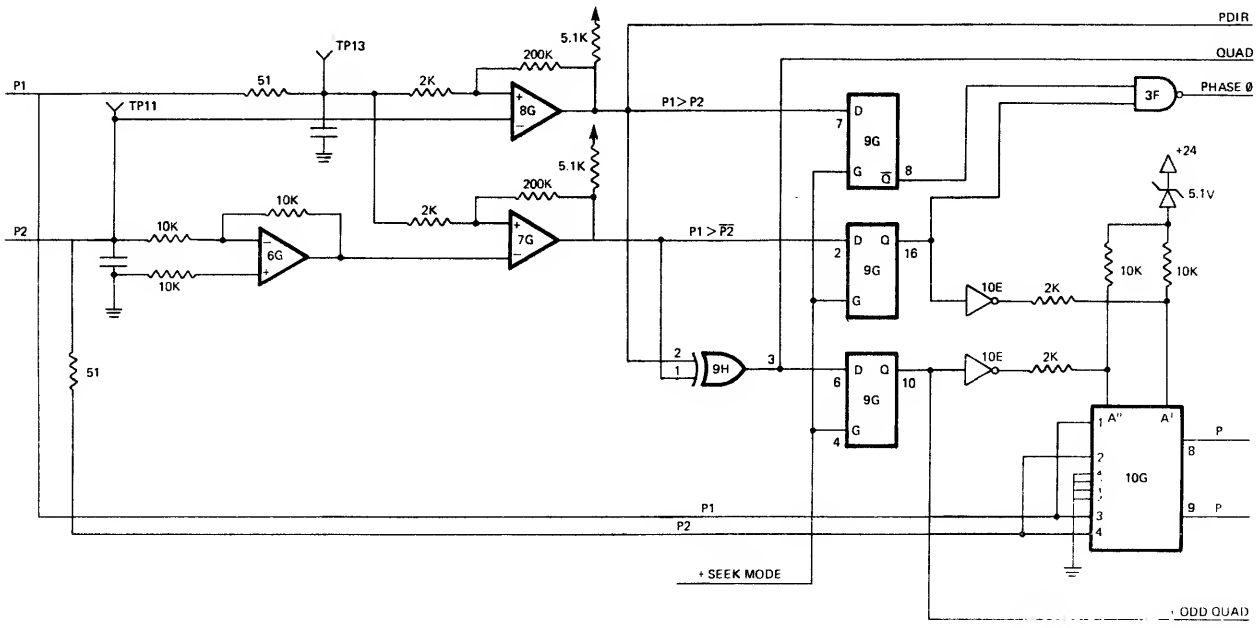


FIGURE 4-23
COARSE TRACK POSITION GENERATION

Figure 4-23 shows the circuitry used in Series 2000 to develop the coarse track position signals. The actual circuitry is found on Figure 6-4, page 6-6, location A and B, 4 through 8. The transducer signals P1 and P2 are compared by comparator 8G whose output is HI when P1 is greater than P2. Amplifer 6G inverts signal P2 to $\overline{P2}$ and comparator 7G produces a signal that is HI when P1 $>\overline{P2}$. When the processor commmands seek mode, the gate input to the 9G F/Fs is true and the Q outputs follow the D inputs. The Q outputs, 9G-16 and 10, are applied through open collector inverters 10E and 5B as address bits to analog switch 10G.

Open collector inverters are used because the MOS analog switch requires the address line voltage to be above 15 volts. CR23, C91, R154, R153, and R152 are used to develop a 19V supply voltage for the address lines. Flip-flops 9G-8 and 9G-16 are ANDED at gate 3F to produce the - PHASE 0 signal which occurs once every four tracks and is used in conjunction with the - T ZERO signal from the transducer to produce the TRACK 000 signal to the interface. Refer to Figure 6-3, page 6-5 location D4 through 8. The -T ZERO signal is applied to comparator 8H whose output is LO whenever the track zero photo cell sees no light. This normally occurs at about track 2 or 3. When the - PHASE 0 signal goes LO, gate 7H outputs the TRACK 000 signal to driver 5J and to the processor.

The output of exclusive OR 9H produces a signal called QUAD. The processor uses the state changes of QUAD as the indication that the heads have crossed a track. The level of signal PDIR (P1 > P2) is sampled by the processor when on track and stored. When the processor commands the actuator to move, PDIR is sampled when QUAD changes state and the new level of PDIR will be compared to the old to determine if the actuator is moving in the correct direction.

9G-10 is input to the processor via multiplexer 7F-13. This signal is used to set the proper polarity for the thermal offset voltage. Analog switch 10G outputs either the linear portion of P1 and P2 or ground, as determined by the applied address. Addresses 00 and 01 switch the linear portion of P2 to pin 8 and ground to pin 9. Addresses 10 and 11 switch the linear portion of P1 to pin 9 and ground to pin 8.

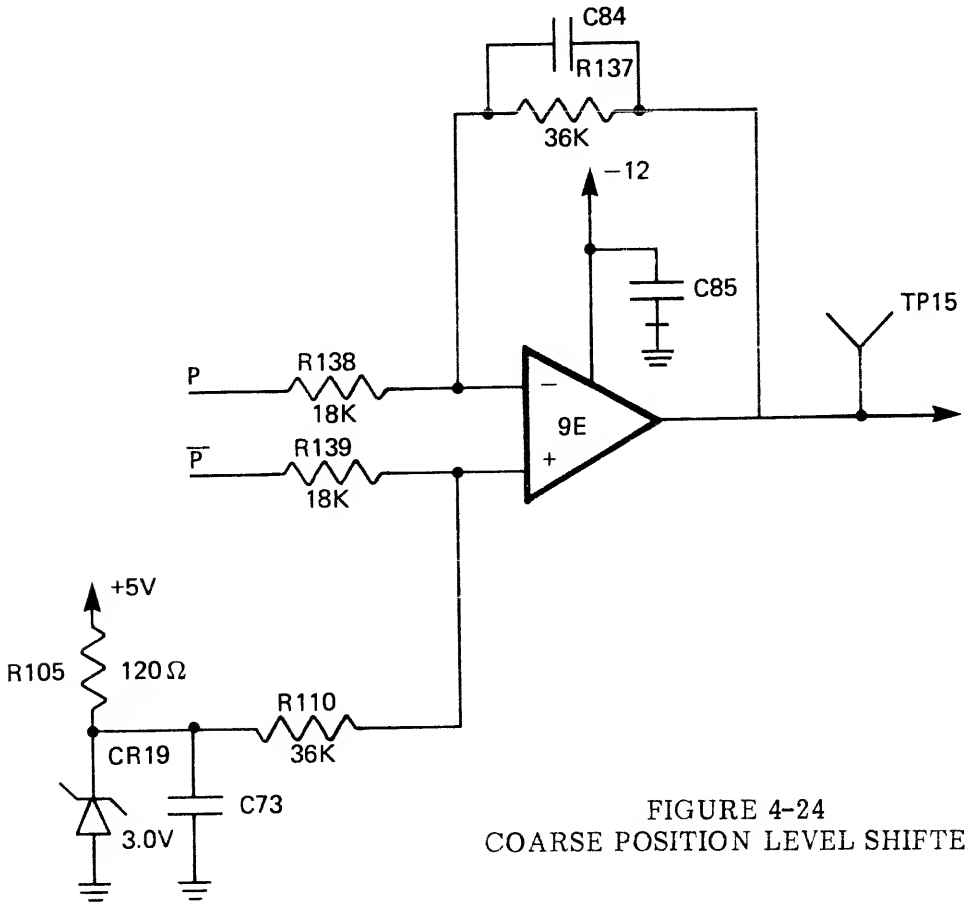


FIGURE 4-24
COARSE POSITION LEVEL SHIFTER

These outputs are applied to differential amplifier 9E where the ground reference of the signals is offset to +3V, generated by R105, zener diode CR19, and capicator C73. The offset amplifier output is then used at the actuator drive summing junction as an indication of coarse track position. Since the point where the amplifier output crosses the +3V reference corresponds to a peak of either P1 or P2 this level is the scale track center. Therefore a +3V output from 9E will position the heads at the scale track center. An output of either 4V or 2V will position the heads 1/2 track off the scale track center, with the more positive voltage positioning toward the outside,and the more negative positioning toward the inside. Figure 4-25 shows the timing relationships of these signals.

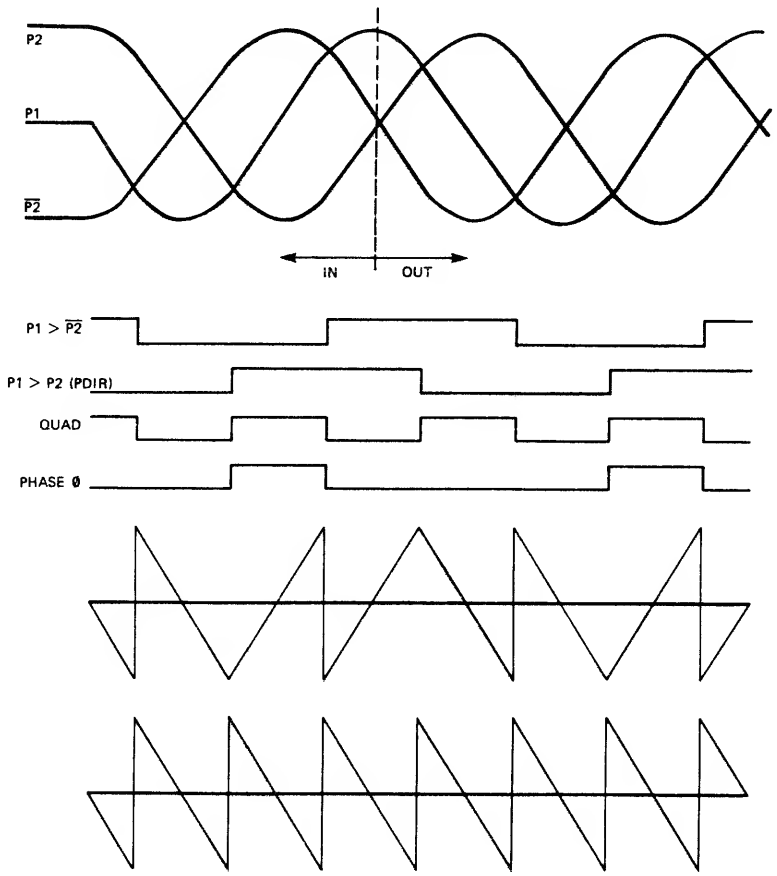


FIGURE 4-25
TRACK POSITION SIGNAL

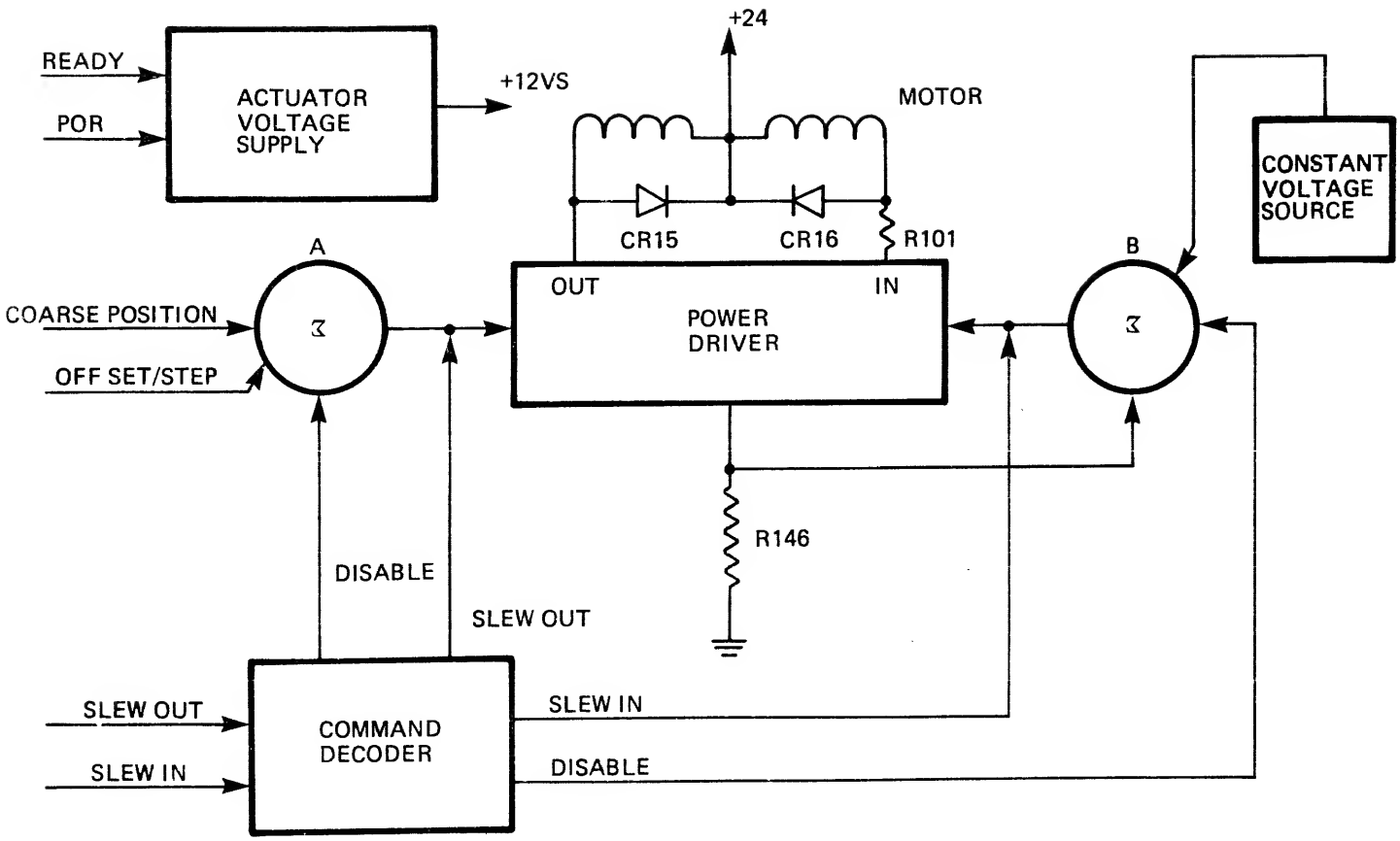


FIGURE 4-26
ACTUATOR CIRCUIRTY BLOCK DIAGRAM

4.3.9 Actuator Drive Circuits

Figure 4-26 is a functional block diagram of the actuator drive circuitry. The actuator drive circuitry consists of the motor. motor power drivers, two summing amplifiers, a command decoder and a gated voltage supply. The gated voltage supply removes power to the actuator during the power on reset and when the drive is not READY. This causes the actuator return spring to pull the head arms over the landing zone to prevent damage to the data areas of the media. The power drivers provide the current to the actuator coils. The actuator has two coils connected to +24V DC, one coil drives the heads in, the other drives the heads out. The processor uses four commands, encoded on the slew lines, to control the actuator: slew in, slew out, coast,and on track. The command decoder decodes the state of the slew lines to provide the drive signals to the power drivers and the disable signals to the summing amplifiers.

If the command is slew, in or out, the summing amplifiers are disabled and the proper side of the power driver is driven. The coast command removes drive from the power driver and also disables the summing amplifiers. The on track command allows the summing amplifiers to control the power driver.

The output of summing amplifier A controls current flowing through the "out" driver by summing the coarse position voltage and the offset voltage. Both drivers have a common resistor, R146 that senses the total actuator current and is one input to summing amplifier B. The other input is a reference voltage. When the resistor voltage matches the reference voltage the "in" drive current is correct, the total actuator current is correct, and the heads are held in position. If the output of summing amplifier A causes the "out" drive to decrease, amplifier B senses the drop in total current and increases the "in" drive current causing the heads move in. When the coarse position voltage matches the offset voltage summing amplifier A increases the "out" drive current to stop the head motion. Summing amplifier B senses the increase and reduces the "in" drive current causing the heads stop. This method of moving the heads is used when the seek distance is short (less than eight tracks) and to offset the heads for thermal compensation.

Figure 4-27 is a partial schematic of the actuator drive circuits. The actual circuitry is found on page 6-7, Figure 6-5, locations A and B, 1 through 8. Darlington transistors Q7 and Q8 are the power drivers for the actuator coils. The coils are protected from high induced voltages when power is removed by suppressor diodes CR15 and CR16. Resistor R101 compensates for the force of the actuator return spring by limiting the "in" drive current. Open collector inverters 10E, 5B and gate 2H are the command decoder. Amplifiers 9D and 8D are the summing amplifiers, A and B respectively. The inputs to amplifier 9D are coarse position voltage at TP15 and offset or step voltage at TP12. When the heads are on track both slew inputs are LO, NAND 2H and inverter 10E reverse bais diodes CR21 and CR22 disabling the slew outputs from inverters 10E, pins 2 and 4. Inverters 5B and 10E, pin 6 allow the amplifiers to control the actuator current. Assuming no thermal offset is required the processor will output a +3 volts on the offset line. When the coarse position voltage equals +3V amplifier 9D is balanced and outputs some nominal voltage. (The coarse position voltage is +3V when the heads are on the scale track center - see paragraph 4.3.8.) This nominal voltage causes current to flow through the "out" transistor, Q7. If the voltage drop across R146 matches the voltage provided by divider R104 and R106 the current flowing through Q8 is correct and the actuator is held on track in a balanced state.

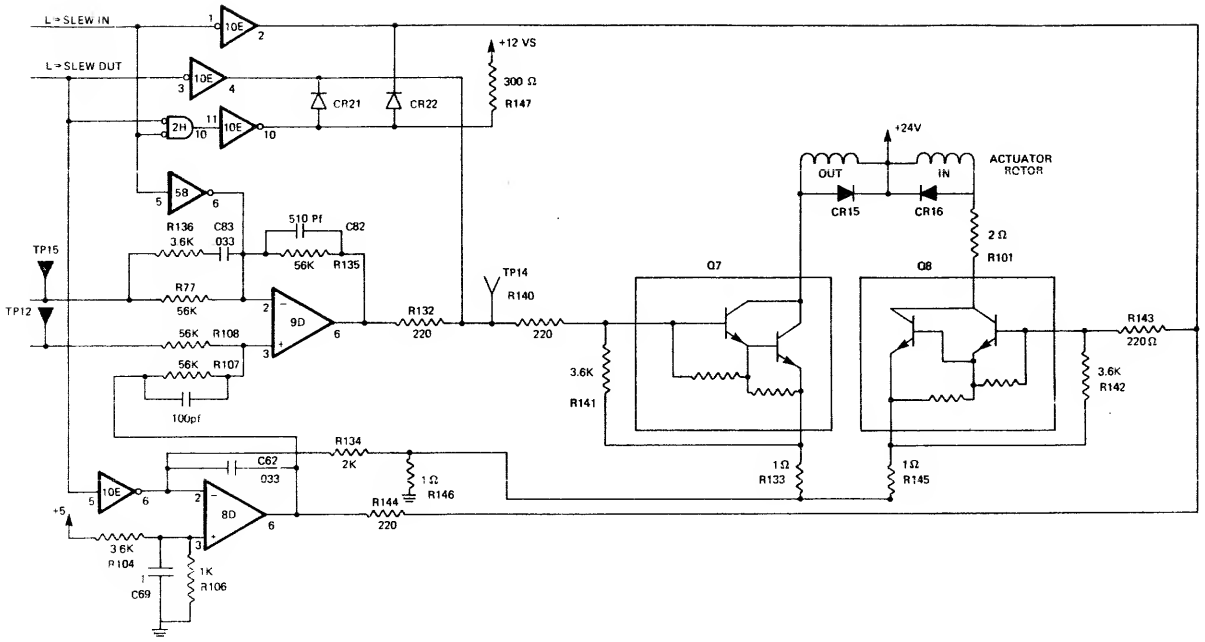


FIGURE 4-27
ACTUATOR CIRCUIT

If the drive is above or below its normal operating temperature the processor will command an offset voltage. This offset voltage will be applied to amplifier 9D at TP12. Amplifier 9D becomes unbalanced and outputs a voltage that increases or decreases the current through Q7. Current decreases in Q7 to move the heads in, and increases in Q7 to move the heads out. If the direction is in, less current flows through R146, amplifier 8D sees less voltage at pin 2 and outputs a more positive drive voltage causing Q8 to conduct harder moving the heads in. As the heads move the coarse position voltage changes, when it equals the offset voltage amplifier 9D again becomes balanced. The amplifier output returns to nominal increasing the current through Q7 counteracting the "in" drive current. The increase in total current is sensed by amplifier 8D and its output goes less positive removing the "in" drive current and the actuator stops at the new position. In this manner, the heads are held on the actual track center over a wide temperature range. In fact the heads can be moved up to one-half track either side of scale track center.

If the drive is commanded to move in or out fewer than eight tracks the processor will use a step voltage to command the move. This is accomplished by forcing the offset voltage to be greater than the one-half track offset voltage. This causes amplifier 9D to become unbalanced as above and the heads move as commanded. In this case however, the coarse position voltage cannot match the offset voltage so the heads continue to move from track to track until this larger than normal voltage (step voltage) is removed and the offset voltage is reapplied. This allows the coarse position voltage to match the offset voltage and the heads stop on the desired track.

If the drive is commanded to move more than eight tracks the processor will command a slew in the desired direction. The desired slew line will remain LO and the other line will be driven HI, gate 2H outputs a LO and 10E, pin 10 allows diodes CR21 and CR22 to become forward biased. This provides a +12V drive to the base of the selected power driver and the actuator moves with maximum torque. To prevent the opposing motor driver from interfering with the action of the selected driver the amplifier associated with the opposing driver is disabled by a LO output from either inverter 10E or 5B, pin 6. During a slew the processor monitors the actuator speed via the QUAD signal and, if it is too high, coast is commanded. Coast causes both slew inputs to be HI disabling both amplifiers and placing a LO on the bases of both power drivers. The drivers turn off and no current is supplied to the actuator coils. When the speed drops to a proper level the desired slew line is again driven LO and the action continues until it is time to stop. At this time the processor reverses the levels of the slew lines and the actuator attempts to reverse direction. This dynamic braking action causes the actuator to slow and eventually stop at the target track. Once again on track is commanded, offset applied, and the heads centered on the actual track center of the target track.

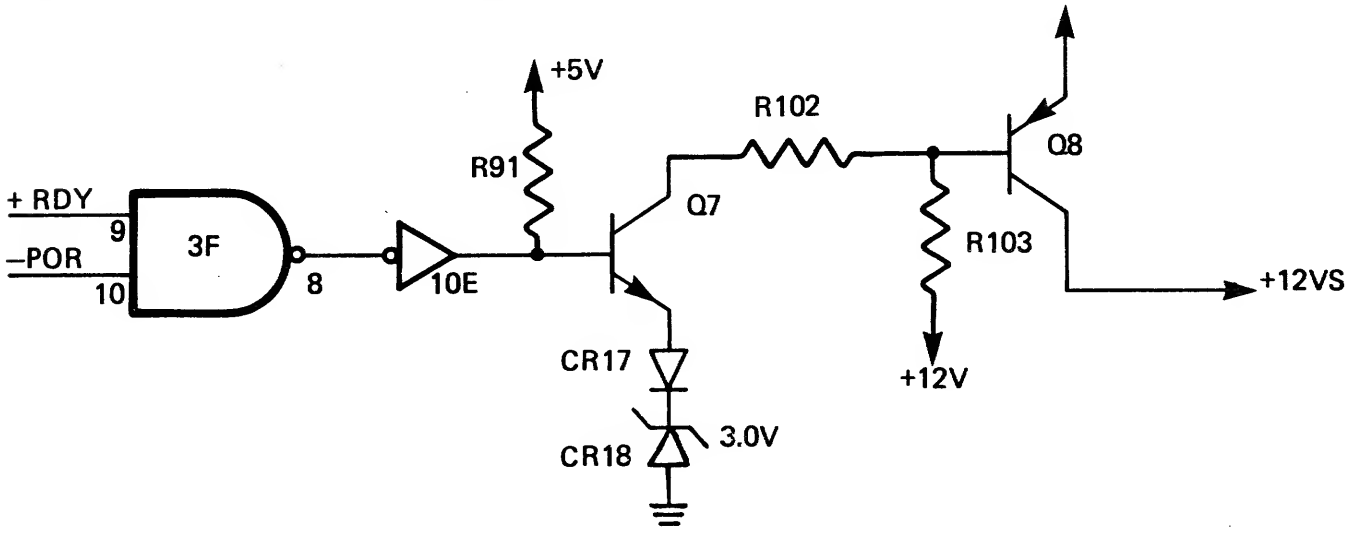


FIGURE 4-28
ACTUATOR POWER SOURCE

The positive supply voltage for both amplifiers and the slew voltage is supplied from a gated voltage source. Figure 4-28 illustrates this source. Transistor Q8 provides +12V as +12VS if it is turned on. Base drive to turn Q8 on is supplied when Q7 is turned on. Transistor Q7 turns on if the +5V supply is greater than +3.5V and NAND gate 3F is enabled. NAND 3F inputs are -POR and +READY. The circuitry then will provide operating voltage for the actuator circuits when all the following conditions are met:

1) +24V is present (since +12V is regulated from +24V)

2) +5V is greater than +3.5 (set by CR18, CR17 in the emitter of Q7).

3) Power on reset has passed (3F-10).

4) READY is HI (3F-9)

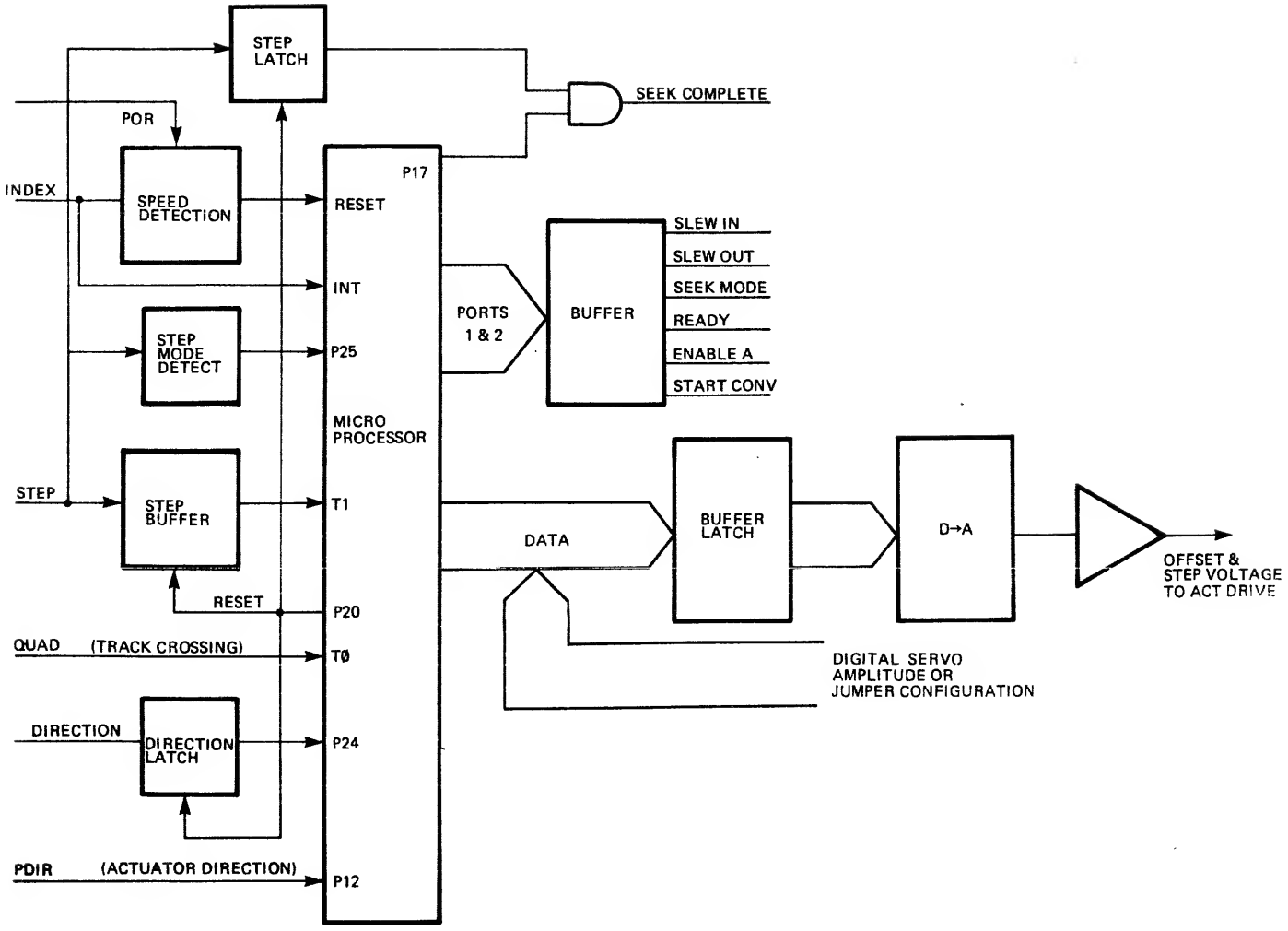


FIGURE 4-29
MICROPROCESSOR CIRCUITRY BLOCK DIAGRAM

4.3.10 Microprocessor Circuits

A block diagram of the microprocessor and its associated circuitry is illustrated on Figure 4-29. The Series 2000 uses a single chip microprocessor with proprietary and copyrighted firmware to control the position of the drive heads. In addition the processor provides a diagnostic mode that tests the drive's ability to seek. The processor contains an eight bit CPU, ROM and RAM memory, two eight bit I/O ports, an eight bit timer/counter, an eight bit data bus and two testable input pins. Used in conjunction with the processor are; an eight bit latch used to latch the offset word, an eight bit D to A converter, some buffers to provide extra drive capability, a disk speed monitor, a step mode detector, a step direction latch and a step buffer.

When power is applied to the drive the power on reset (POR) holds the disk speed monitor reset, which in turn holds the processor reset. Once POR is removed and the disks are 70% up to speed the disk speed monitor releases the processor reset and the internal program starts. The processor will measure the time between index pulses and if the disks are greater than 90% up to speed it activates the READY line and starts the recalibrate sequence. When the recalibrate sequence is completed it activates SEEK COMPLETE. The processor then waits for one of three events to occur:

1) Index

2) Diagnostic jumper (E4) in place

3) Step pulses

When index occurs, the processor will command the sample and holds to save the servo amplitudes, the A to D converter to convert these amplitudes to digital values, read the converted data, and apply the computed offset via the D to A converter to the actuator drive circuit. This function may be disabled for test purposes by installing jumper E3.

If the diagnostic jumper is in place the processor starts the diagnostic seek program. This program commands the actuator to seek in a diagnostic mode while using an internal track number register to monitor track position. If this track register indicates track 000 and the drive is not at track 000 or if the drive indicates track 000 and the register is not at track 000, the processor stops the actuator until reset. The diagnostic seek mode is:

1) Start at track 000

2) Seek to track 001

3) Seek to track 000

4) Seek to track 002

5) Seek to track 000

6) Seek to track 003

7) Seek to track 000

8) Continue until all tracks are hit, then repeat.

If the diagnostic jumper (E4) is not installed and step pulses are received, the processor looks at the step mode detector to see if the steps are coming in burst mode or normal mode. If burst mode, the step buffer divides the number of steps by four and inputs the divided steps to the internal counter of the processor. When all steps are input the processor resets the step divider and direction latch and starts the seek. If the steps come in normal mode, the processor immediately resets the step divider and direction latch and starts the seek. To seek, the processor commands slew or outputs the step word and monitors the QUAD and PDIR inputs. As the heads move the QUAD input toggles as each track is crossed, PDIR is monitored to to ensure the actuator is moving in the desired direction. When the correct number of tracks have been crossed the processor commands on track and allows the actuator time to settle. The offset word is then output to the D to A converter where it becomes the offset voltage and is applied to the actuator drive circuit. When the heads have settled the processor activates the SEEK COMPLETE line.

Figure 4-30 is a schematic of the processor and its associated logic elments. The actual circuitry is found on page 6-7, Figure 6-5, locations C and D 1 through 8.
The speed monitor 3E is a 27 ms retriggerable one-shot that is triggered by index and held reset by - POR. When the disks are rotating at 3000 RPM index will occur every 20 ms, and the one-shot output remains HI. If the disks slow down it times out, or if DC power is removed it is reset; in either case it's output goes LO resetting the processor which drops READY removing actuator power.

Burst mode detector 4E is another retriggerable one-shot with a period of 600 usec. As long as step pulses arrive faster than every 600 usec its output will remain LO. The processor senses this condition at Port 2, bit 5.

Step direction is latched by one section of the quad flip-flop, 9F and is sensed by the processor at Port 2, bit 4. A second flip-flop of 9F is used to drop SEEK COMPLETE via gate 5H as soon as a step pulse is received. The remaining two flip-flops of 9F are configured as a two bit counter with the addition of exclusive OR 9H. The counter divides the number of step pulses received by four, and causes the internal eight bit counter to increment with each count of four. This way 512 steps can be stored in the internal counter, and the step rate can be faster than the 15 usec maximum count rate.

Hex inverter 5E is connected to some of the port outputs to provide extra drive current on those signals that require it.

Octal latch 7E latches the output of the data bus for use by the eight bit D to A converter 7D. The latched data will be either the thermal offset word or the step word. The output of the D to A converter is a current that is porportional to the input binary value. This current is converted to a voltage by amplifier 8E and applied to the actuator drive circuits. The offset voltages are between +2V and +4V and the step voltages are less than +2V or greater than +4V.

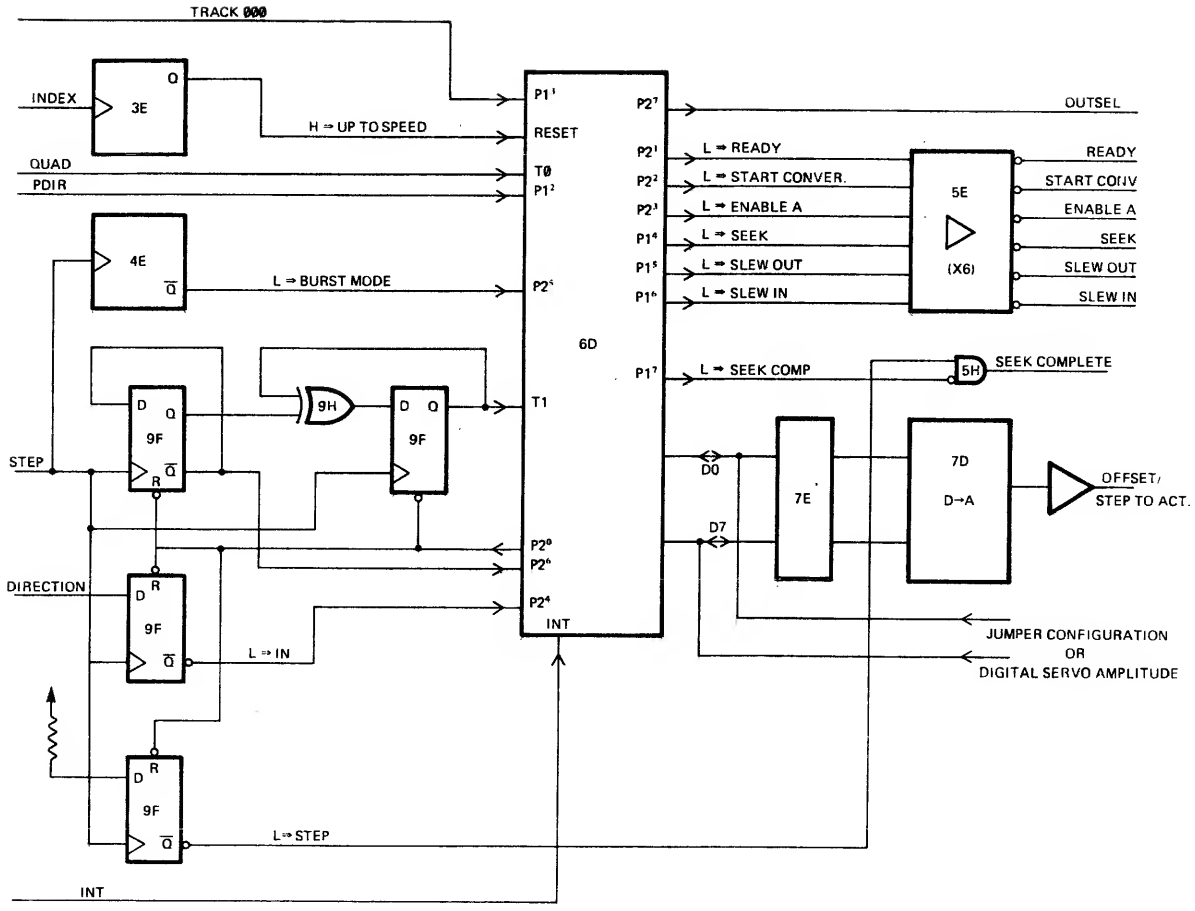


FIGURE 4-30
MICROPROCESSOR CIRCUITS

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SECTION 5

MAINTENANCE

5.1 GENERAL INFORMATION

A high degree of reliability has been achieved in the Series 2000 through the simplicity of its mechanical design and the extensive use of microelectronics. The Series 2000 is designed for fast, easy subassembly replacement with no adjustments, greatly reducing the amount of downtime for unscheduled repairs.

5.2 MAINTENANCE PRECAUTIONS

Observing the following precautions during service activity will help avoid damage to the Series 2000 and personal injury to the service technician.

1. Do not transport the drive without the actuator and spindle locks engaged.

2. Avoid harsh shocks to the drive especially when the spindle and actuator locks are disengaged or when the drive is operating.

3. Do NOT open or remove the plastic bubble or its seals unless the drive is in a Class 100 clean environment. See the optional Section 8 of this manual for Sub-bubble repair details.

4. Potentially hazardous AC voltage is present on the underside of the drive for the spindle drive motor.

5. Exercise caution when operating the drive with the cabinet and drive belt shield removed. Stay clear of the belt motor and spindle pulley.

6. Do not lift the drive by the face plate or the PCBA.

5.3 PREVENTATIVE MAINTENANCE

The Series 2000 does not require any preventative maintenance.

5.4 MAINTENANCE LEVELS, TOOLS, EQUIPMENT AND SPARES

5.4.1 Levels of Maintenance

Corrective maintenance on the Series 2000 requires certain minimum levels of technical expertise and facilities. Capabilities in this area will vary greatly from user to user. Maintenance procedures for the Series 2000 are categorized into two levels. The first level involves on-site exchange of subassemblies or the drive itself. The second level involves service center and/or factory repair or refurbishment of assemblies and the printed circuit board.

5.4.1.1 Level 1 - Unit replacement, circuit board exchange, external subassembly replacement, or drive belt replacement.

5.4.1.2 Level 2 - Level 1 plus major disassembly and refurbishment of the drive and repair of circuit boards.

NOTE

The user's service activity should be limited to only Level 1 procedures during the warranty period. The Quantum warranty is null and void when any Level 2 procedure has been attempted. In addition, no sub-bubble repairs are authorized. All time and material required to restore the drive to working order will be billed at prevailing rates.

5.4.2 Tools, Equipment and Spares

5.4.2.1 Level 1

The following listed items should be available to personnel providing Level 1 maintenance on the Series 2000.

An aasortment of hand tools adequate for electronic/mechanical repair
One drive control PCBA. Quantum part number 20-20000
One AC drive motor. See Table 5-1 for part numbers
One drive power transistor assembly. Quantum part number 75-40067
One drive belt. See Table 5-1 for part numbers.
One torque driver handle, preset to 22 in.-lbs, with a #8 Allen tip, a #2 Phillips tip, and a 3/32 hex socket tip.

5.4.2.2 Level 2

The items listed below, plus those listed for Level 1 should be available to persons performing corrective maintenance and/or repair of the Series 2000 at Level 2.

- Oscilloscope, vbw 100 MHZ, vds 10 mv/cm, sweep speed 50 ns/cm
- Exerciser QTE-1 Drive exerciser. Quantum part number 76-95079.
- Servo Writer, QTE-2. Quantum part number 76-95029.
- Media Scanner QTE-X. Quantum part number 76-95019
- Final tester QTE-X or equilivlent. Quantum part number xx-xxxxx
- Transducer Adjust Station, QTE-4. Quantum part number 76-95027
- Power Supply, QTE-3. Quantum part number 76-95053x
- Digital volt meter. Fluke D-800 or equivilent.

Sub-bubble repair requires the additional tools and equipment specified in optional Section 8 of this manual.

5.5 AC INPUT VOLTAGE AND FREQUENCY CONVERSION

5.5.1 Frequency Conversion

The AC drive motor used in the Series 2000 is able to operate on either 50 or 60 HZ at its rated voltage. The rotational speed of the motor is dependant on its input frequency and is slower at 50 HZ. To keep the spindle speed constant with the different motor speeds, two sizes of drive motor pulleys are used. Along with these two pulley sizes there are two different drive belt sizes. Table 5-1 lists the part numbers of these parts.

Table 5-1
Voltage and Frequency Parts

POWER		PART NUMBERS			
Voltage	Frequency	Motor	Pulley	Belt	Motor/Pulley Assy.
110 VAC	60 HZ	73-40109	40-40015	50-40000	73-40226
110 VAC	50 HZ	73-40109	40-40032	50-40001	73-40227
220 VAC	60 HZ	73-40111	40-40015	50-40000	73-40228
220 VAC	50 HZ	73-40111	40-40032	50-40001	73-40229

To change the drive from operating at one frequency to the other proceed as follows:

1. Select the pulley and belt for the desired frequency from Table 5-1.
2. Remove all power and interface cables from the drive and place the drive on the work surface.
3. Engage the actuator lock.
4. Remove the cabinet assembly by removing the 3 Phillips head screws on the bottom of the cabinet hold the assembly to the shock mounts.
5. Remove the capacitor clamp.
6. Remove the old drive belt.
7. Remove the old pulley by loosening the two Allen drive set screws using a #8 Allen wrench.
8. Install the new pulley. Ensure that one of the set screws will match the flat side on the shaft and the pulley is seated down so that there is .030 inches clearance between the top of the motor and the pulley.

NOTE

A 50 HZ pulley is larger than the 60 HZ. A 50 HZ belt can be identified by the white square on one side.

9. Tighten the set screws to 22 in.-lbs.

10. Install the new belt.

11. Reinstall the capacitor clamp.

12. Reinstall the cabinet assembly

13. Reinstall the drive and test as required.

5.5.2 Voltage Conversion

The Series 2000 AC drive motor will only operate within one of two voltage ranges. The motor ranges are 90 to 127 VAC, and 180 to 253 VAC. To convert from one range to the other it is necessary to exchange the motor with one having the desired voltage range. Table 5-1 lists the part numbers of the two motor assemblies. To change motors proceed as follows:

1) Select the required motor assembly from Table 5-1.

2) Remove all power and interface cables from the drive and place the drive on the work surface.

3) Engage the actuator lock.

4) Remove the cabinet assembly from the drive by removing the 3 Phillips head screws on the cabinet.

5) Remove the belt guard by removing the two Phillips head screws.

6) Remove the drive belt.

7) Remove the AC input connector J4 from its bracket.

8) Disconnect the AC ground wire from the chassis. The wire runs from the AC Motor to the top side of the base casting where it is secured by a Phillips screw.

9) Remove the motor leads from the tywrap hold downs by cutting the tywraps. Be careful not to damage the wires.

10) Remove the motor by loosening and removing the 3/32 inch mounting nuts.

11) Installation of the new motor is the reverse of the foregoing steps.

12) Torque the mounting nuts to 22 in.-lbs.

PICTURE NOT AVAILABLE AT TIME OF PRINTING

FIGURE 5-1
SERIES 2000 BOTTOM VIEW

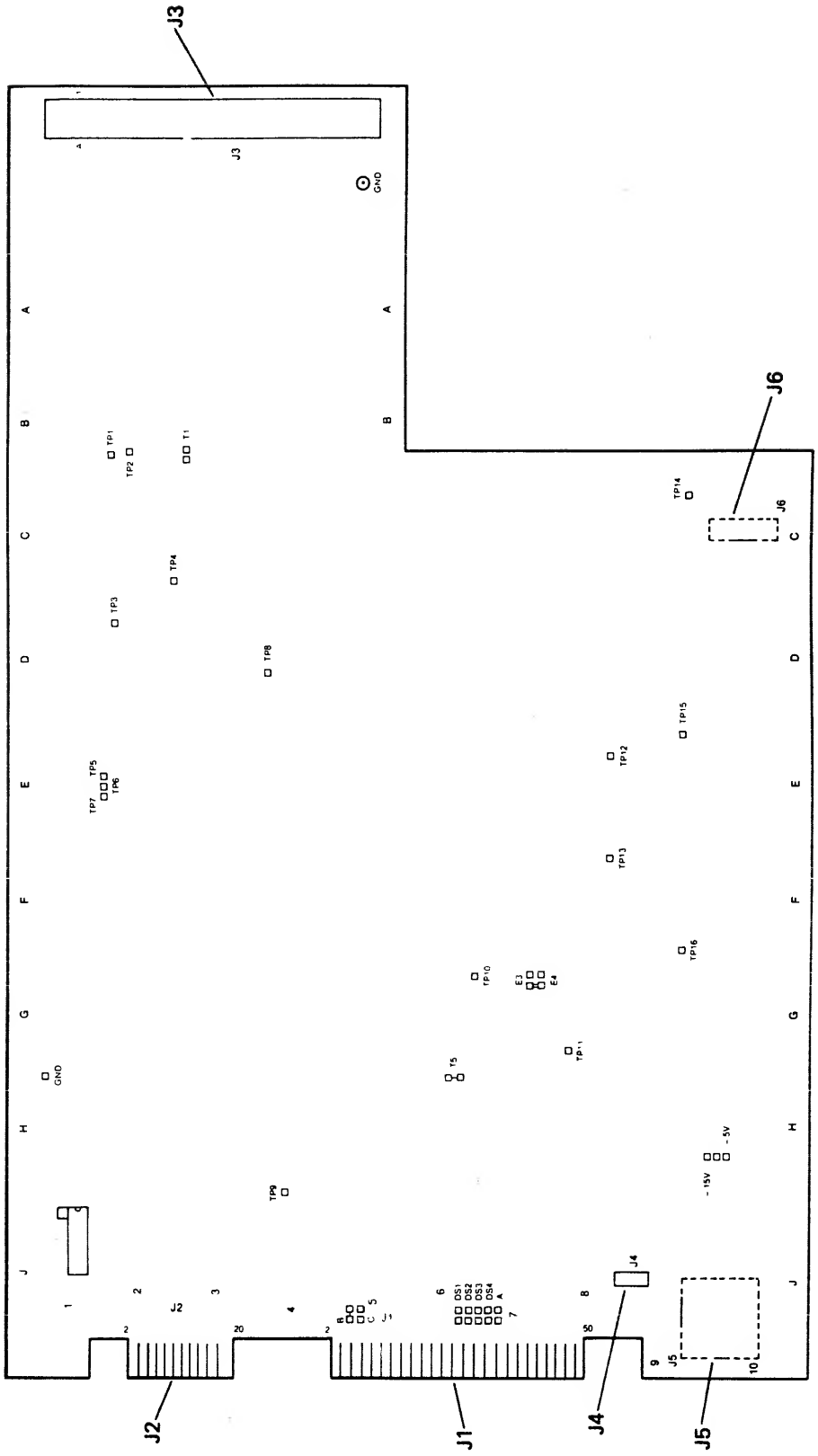

FIGURE 5-2
CONNECTOR LOCATIONS

5.6 REMOVAL AND REPLACEMENT

5.6.1 Drive Control PCB

1) Remove the interface and DC power cables, the drive transistor cable and the index cable. See Figure 5-3 for the connector locations.

2) Remove the 4 Phillips head screws holding the PCB to the drive.

3) Gently lift the PCB off the transducer connector at the narrow end of the PCB.

4) Install the new PCB in the reverse order of the foregoing steps.

5) Torque the hold down screws to 22 in.-lbs.

5.6.2 Drive Power Transistor Assembly

1) Remove all power and interface cables from the drive and place the drive on the work surface.

2) Remove the cabinet assembly from the drive.

3) Gently remove the drive transistor cable connector from the control PCB.

4) Remove the belt guard and drive belt from the drive.

5) Remove the drive transistor leads from the tywrap hold downs.

6) Remove the AC connector J4 from the drive transistor mounting bracket.

7) Remove the drive transistor assembly by removing the hold down screw. Refer to Figure 5-2 for screw location.

8) Install the new power transistor assembly in the reverse order of the foregoing.

9) Torque the hold down screws to 22 in.-lbs.

5.7 DRIVE CONTROL PCBA CHECKOUT

5.7.1 General Discussion

Drive problems that are isolated to the Drive Control PCBA may be further isolated to the malfunctioning area by using the flowchart on the following pages.

5.7.2 Flowchart

Figures 5-3 through 5-6, are intended to be used as generalized guide for testing and troubleshooting the drive control PCBA of the Series 2000. The flowchart requires test equipment that will allow the user to: seek to, and write or read on selected tracks and heads. The user should also be skilled in both analog and digital troubleshooting techniques.

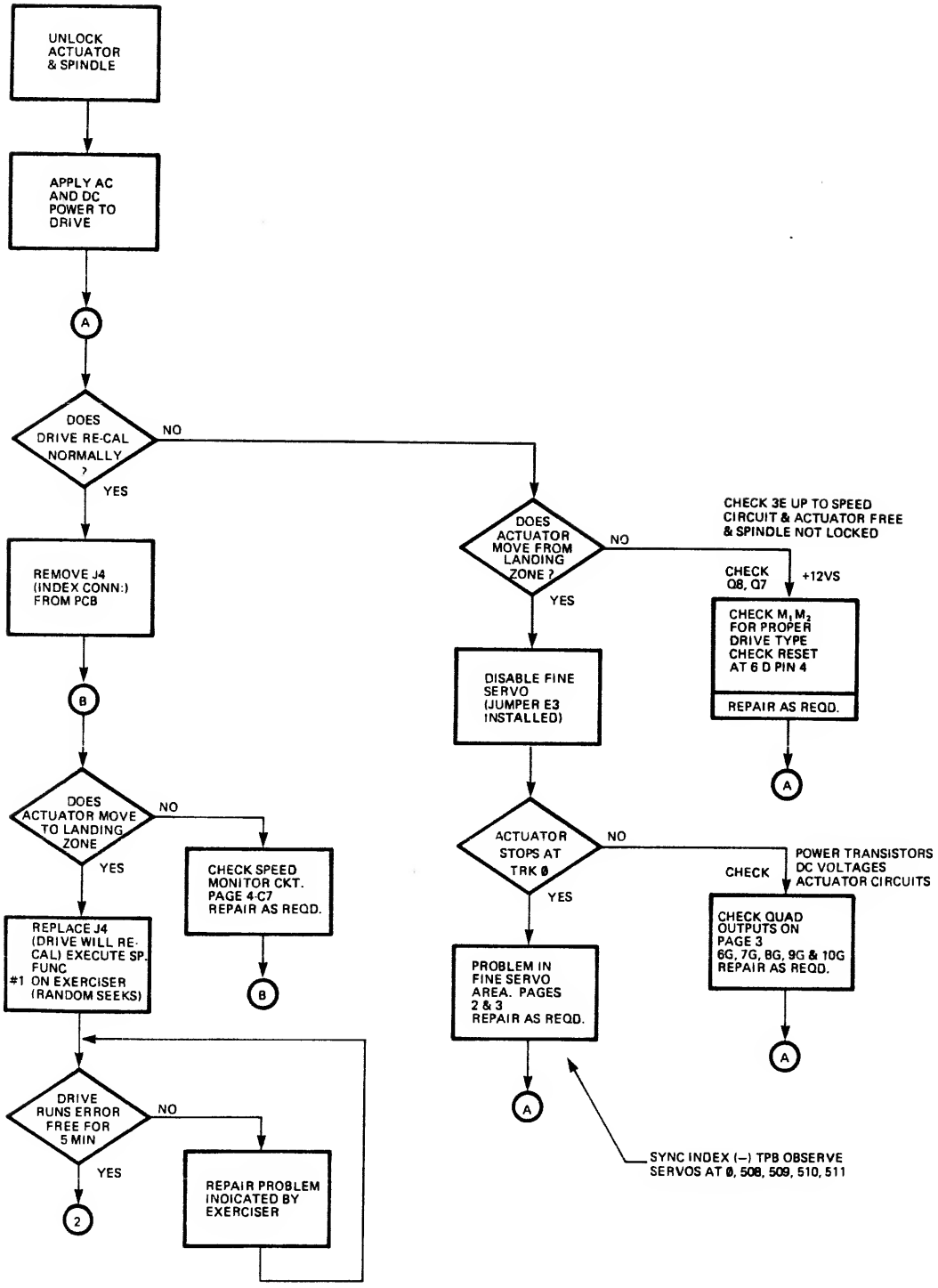

FIGURE 5-3
DRIVE CONTROL PCBA CHECKOUT

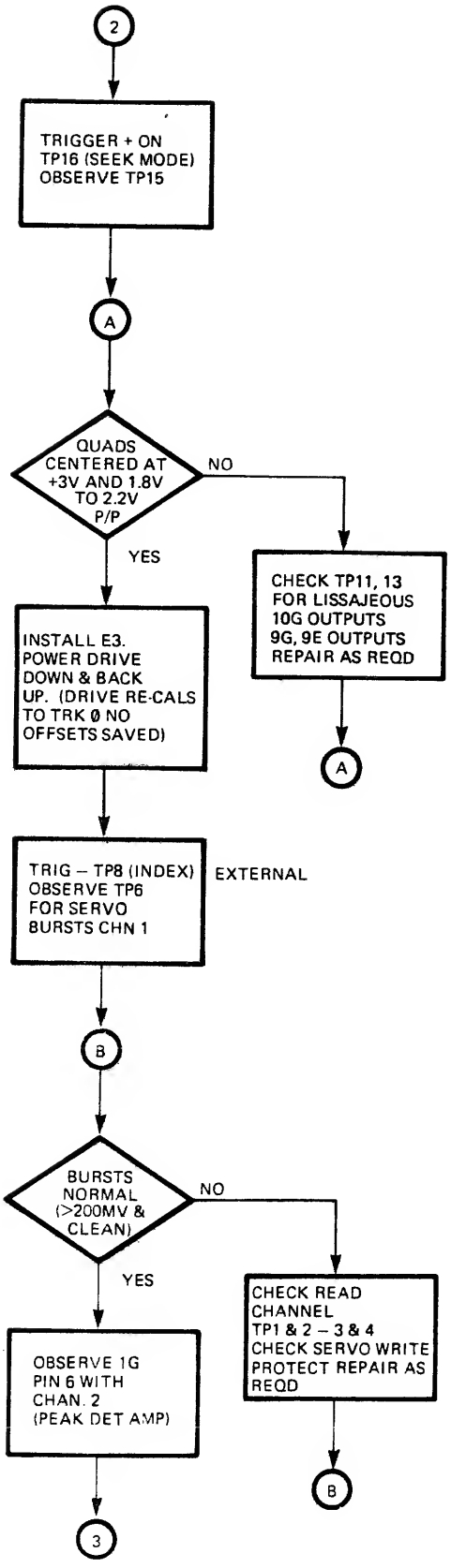

FIGURE 5-4
DRIVE CONTROL PCBA CHECKOUT

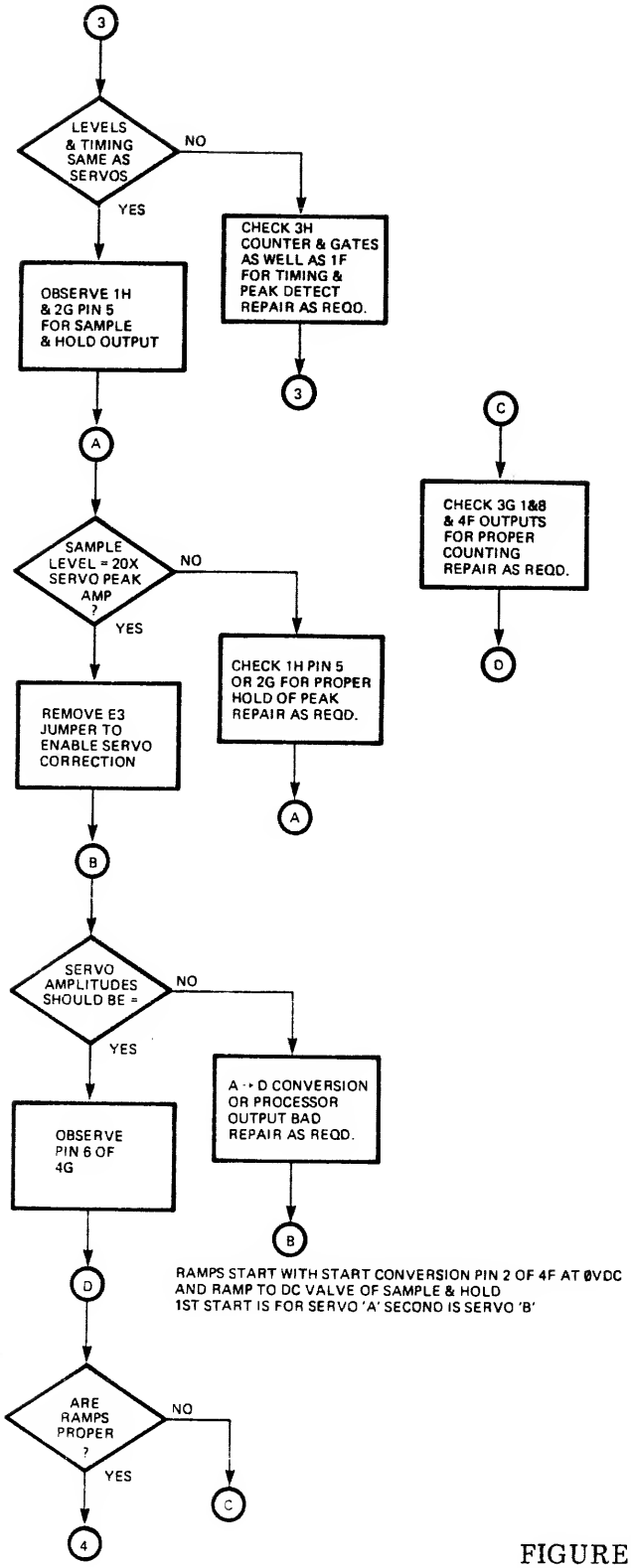

FIGURE 5-5
DRIVE CONTROL PCBA CHECKOUT

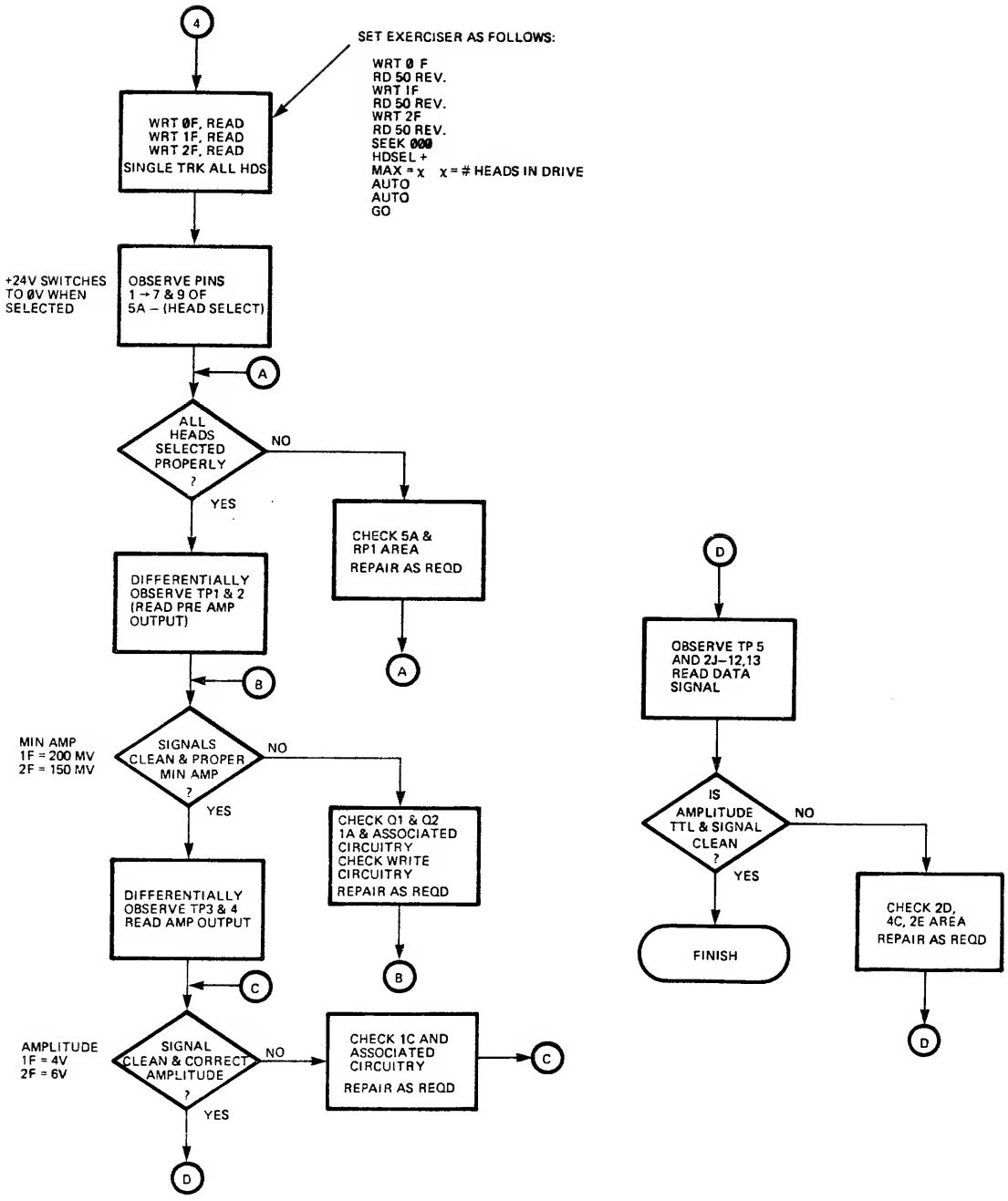

FIGURE 5-6
DRIVE CONTROL PCBA CHECKOUT

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SECTION 6

CIRCUIT DIAGRAMS & LOGIC CONVENTIONS

6.1 GENERAL DISCUSSION

Quantum's logic diagrams emphasize the functions performed by the logic elements rather than the kinds of devices used. For example, a NAND gate may appear on a Quantum diagram as either a positive logic AND function with the output inverted (NAND), or as a negative logic OR function with the inputs inverted (NOR). This practice runs contrary to some logic drawing standards which require the use of the NAND symbol for both functions, but aids field service personnel in troubleshooting and system design engineers in understanding the principles of operation of the design.

This functional approach to logic symbology is basic to the logic documentation conventions employed by Quantum. The conventions that govern logic symbology, signal nomenclature, and other drawing standards that may help the reader interpret Quantum logic diagrams, are discussed in the following paragraphs.

6.2 LOGIC SYMBOLOGY

The logic function symbols used in Quantum's logic diagrams conform closely to those set forth in MIL-STD-806 or ANSI Y32.14-1973. Small scale integration (SSI) circuits are represented by their function symbol. Medium scale (MSI) and large scale (LSI) integration devices, such as shift registers, RAMs, ROMs, etc., are represented by rectangles with function labels. Since both positive and negative logic conventions can appear in a single diagram, the unfilled-circle negation symbol specified by MIL-STD-806 or ANSI Y32.14-1973 is used to distinguish between LO true and HI true signals.

Usually, all logic symbols are drawn with inputs on the left and outputs on the right. Some device symbols, such as flip-flops, show inputs and other external connections on the top and bottom of the symbol for clarity. Also, the drawings themselves are usually drawn with major signal flows from left to right, top to bottom. However, drawing layout restrictions occasionally require the reverse of this, and that some symbols be drawn with a vertical orientation.

Figure 6-1 is a sample diagram, drawn to include examples of most, if not all, of the drawing conventions used. Note that in some cases two "grid coordinate" systems are used. One, shown on the perimeter of the diagram, is useful in locating a portion of a circuit or a particular component on the diagram itself, and has no other meaning. The other involves the component identifiers, such as OR gate 4J. The identifier is a "grid coordinate" code for locating that component on its printed circuit board. Further, textual reference to a device, such as a flip-flop, will usually further identify the device by its major output terminal. In the case of flip-flops, the "Q" output is usually used, i.e. FF 6H-9.

6.3 INTEGRATED CIRCUIT DIAGRAMS

These diagrams schematically illustrate the integrated circuits used in this machine. Pertinent information, such as waveforms and truth tables, is also included when appropriate.

(Integrated circuit illustrations not completed at time of printing.)

6.4 CIRCUIT DIAGRAMS

The schematic diagrams which follow the integrated circuit illustrations represent the latest version of each circuit board in current production at the time of preparation of this manual. Listed on the back of each diagram will be found the revision history of those circuits, plus a listing of the solid state components used, and their component designator codes used for locating each device on its circuit board.

There are two important part numbers associated with each circuit board in the Series 2000.

1) The PCB Assembly part number identifies the complete circuit board with components installed. This number is etched onto the top (component) side of the PCBA. The revision letter of the board assembly generally is marked on this side of the PCBA also.

2) The PCB part number (fabrication number) is the part number of the blank PCB without components. This number is etched on the bottom (solder) side of the PCB. The revision letter of the fabrication is also etched on this side

DIAGRAM NOT AVAILABLE AT TIME OF PRINTING

FIGURE 6-1
SAMPLE LOGIC DIAGRAM

80-20000

-REDUCED WRITE I
-HEAD SEL 2⁰
-HEAD SEL 2¹
-HEAD SEL 2²
-DIRECTION IN
-STEP
-WRITE GATE
GJ TERMINATOR 220/330 (SOCKET) BECKMAN 899-5
-REZERO
(P.2) + WR I
-DRIVE SEL 1
-DRIVE SEL 2
-DRIVE SEL 3
-DRIVE SEL 4
GND
ALL ODD PINS
ALL UNUSED EVEN PINS 10, 12, 16, 24, 46, 48, 50, 38
(P.2) - RD DATA
GND
2, 4, 6, 8, 11, 12, 13, 16, 19, 20,
+ TIMING CLK
- TIMING CLK
+ WRITE DATA
- WRITE DATA
(P.3) + INDEX
(P.4) + SK CMPLT
(P.4) + READY

-REDUCE IW (P.2)
+HEAD 2⁰ (P.2)
+HEAD 2¹ (P.2)
+HEAD 2² (P.2)
+DIR IN (P.4)
-STEP (P.4)
-WRITE FAULT
+DR SEL (P.2,3)
-POR (P.4)
-DRIVE SELECTED
-MFM RD DATA
+MFM RD DATA
+WR DATA (P.2)
+WRITE (P.2)

B	0068	1-81	
C	0073	2-81	
D	0075	2-81	
E	0082	3-81	
F	0090	3-81	
G	0096	5-81	
H	0126	6-81	
J	0149	7-15-81	JTH

CONNECTOR REFERENCE SYMBOLS:

- = J1, 50 PIN - SIGNAL I/O CONNECTOR
- = J2, 20 PIN - DATA I/O CONNECTOR
- = J3, 44 PIN - R/W CONNECTOR
- = J4, 3 PIN - INDEX TRANSDUCER CONNECTOR
- = J5, 6 PIN - DC INPUT CONNECTOR
- = J6, 6 PIN - TRANSISTOR DRIVER CONNECTOR

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C98	-
CR23	-
L16	-
Q8	-
R154	R111
TP16	-
VR2	-
RP1	-

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITORS ARE IN MICROFARADS
2. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%
3. ALL DIODES ARE IN4148
4. ALL TRANSISTORS ARE 2N2222A
5. —□ □— INDICATES JUMPER OPTION
6. -□ □- INDICATES NORMAL POSITION FOR SHORTING PLUG.
7. ALL .1μF CAPACITORS ARE +80%, -20%

FAB REV "D" REWORK SCHEMATIC

EC HISTORY		MUST CONFORM TO ENGINEERING SPEC 35000-070		QUANTUM CORPORATION
DATE	NO	MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE SCHEMATIC DIAGRAM Q2000 CONTROL
			LINEAR .XX / .XXX	DETAIL JTH 9-22-80 RELEASED FOR ASSEMBLY
		CASE DEPTH		DESIGN
		HARDNESS	ANGULAR:	APPRO SHEET 1 OF 4 D
		SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX / INSIDE MAX	SCALE 80-20000 EC J

FIGURE 6-2
DRIVE CONTROL SCHEMATIC SHT.1

80-20000

INDEX TXDUCER

(P.3) – PHASE Ø

– T ZERO

(P.4) +SK CMPLT
(P.4) +READY
(P.1) +DR SEL

+24 VDC
+24 RTN
+5 VDC
+5 RTN
–15 VDC/–5VDC
–5 RTN

– RAW INDEX (P. 3)
+ TRACK ØØØ (P. 4)
SK COMP
–TRØØØ
– READY
– SK COMPLETE
+12 VDC
–5 VDC
GND

– TRØØ DETECT

T.P. 10

TP19

LINEAR (P.3)

TP6

TP3
TP4

–RD DATA (P.1)

(P.1) + HEAD 2⁰
(P.1) + HEAD 2¹
(P.1) + HEAD 2²
(P.3) – INDEX
(P.3) + INDEX

(P.1) +WRITE

(P.1) –REDUCE IW

(P.1) +WR DATA

HD CT Ø
HD CT 1
HD CT 2
HD CT 3
HD CT 4
HD CT 5
HD CT 6
HD CT 7

+ WR I (P.1)

R/W 1
R/W 2

FAB REV 'D' REWORK SCHEMATIC

EC HISTORY		MUST CONFORM TO ENGINEERING SPEC 35000-070		QUANTUM CORPORATION
DATE	NO	MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE SCHEMATIC DIAGRAM Q2000 CONTROL
			LINEAR ± XX	DETAIL 7-10-80 9-22-80 RELEASED FOR ASSEMBLY
		CASE DEPTH	± XXX	DESIGN
		HARDNESS	ANGULAR ±	APPRO D
		SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX	SCALE SHEET 2 OF 4
				80-20000 EC J

FIGURE 6-3
DRIVE CONTROL SCHEMATIC SHT 2.

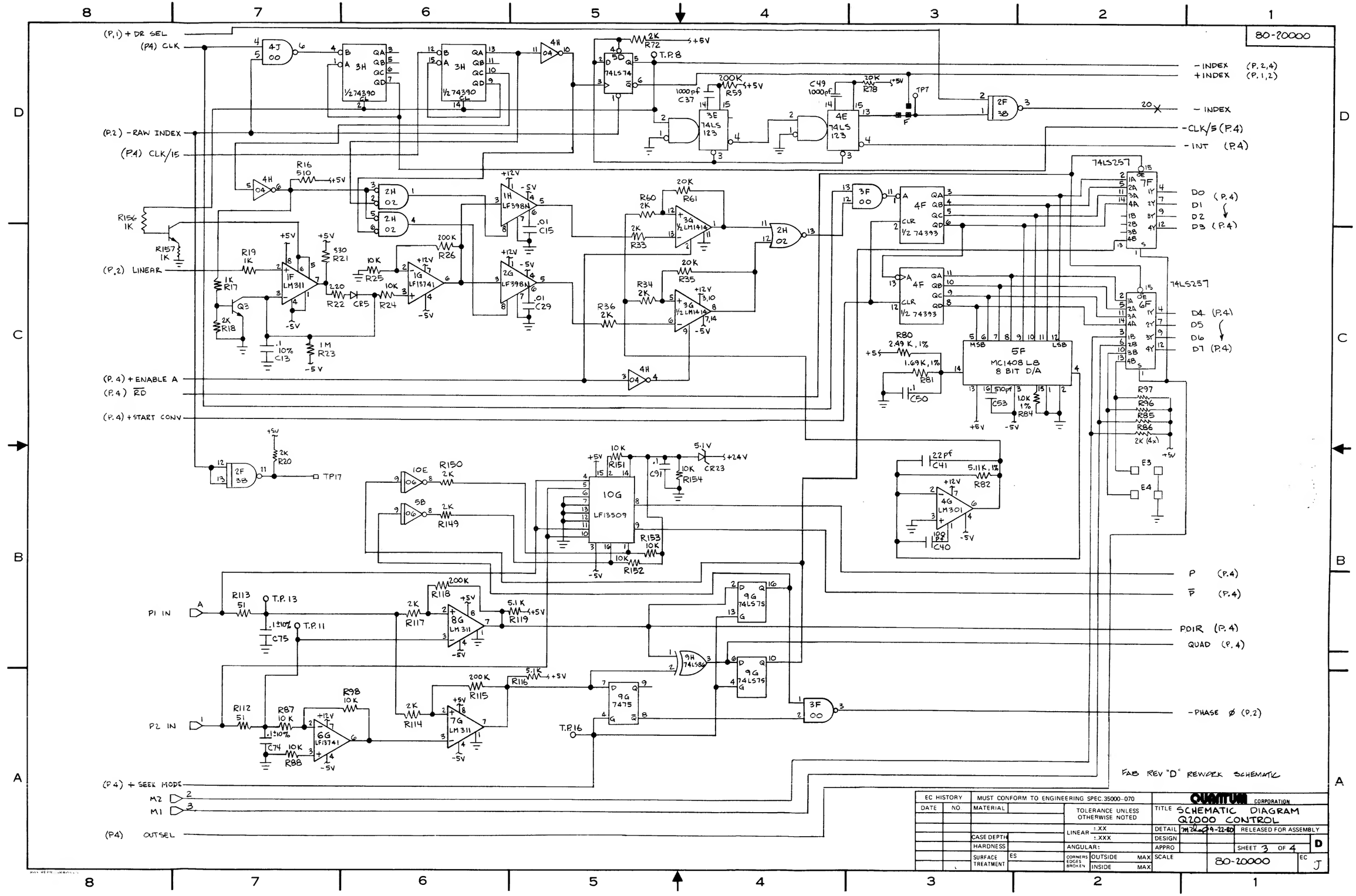


FIGURE 6-4
DRIVE CONTROL SCHEMATIC SHT. 3

80-20000

(P.3) QUAD
(P.3) CLK/5
(P.1) +DIR IN
(P.1) -STEP
(P.3) -INDEX
(P.2) TRACK 000
(P.3) -INT
(P.1) -POR
(P.3) PDIR
(P.3) +INDEX

OUTSEL (P.3)
+5K COMPLT (P.1,2)
+READY (P.1,2)
+START CONV (P.3)
+ENABLE A (P.3)
+SEEK MODE (P.3)
CLK (P.3)
$\overline{RD}$ (P.3)

CLK/15 (P.3)

D0 (P.3)
D1
D2
D3
D4
D5
D6
D7 (P.3)

10 VREF
22, X MTR 1
21, W MTR CT
20, V MTR 2

(P.3) P
(P.3) $\overline{P}$

FAB REV 'D' REWORK SCHEMATIC

EC HISTORY		MUST CONFORM TO ENGINEERING SPEC 35000-070		QUANTUM CORPORATION	
DATE	NO	MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE SCHEMATIC DIAGRAM Q2000 CONTROL	
			LINEAR: .XX / .XXX	DETAIL	RELEASED FOR ASSEMBLY 9-22-80
		CASE DEPTH		DESIGN	D
		HARDNESS	ANGULAR:	APPRO	SHEET 4 OF 4
		SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX / INSIDE MAX	SCALE	80-20000 EC J

FIGURE 6-5
DRIVE CONTROL SCHEMATIC SHT. 4

RP2-A → RP2-D TRIM RESISTOR ARRAY PN

RP1 = 4.7K R-PACK, 16PIN DIP.

ALL AMPLIFIERS : LF347B

ALL RESISTORS 1/4W, 5% (UNLESS OTHERWISE NOTED)

80-20010			
REV	EC	DATE	SIGN
A	0031	11-80	
B	0043	12-80	
C	0098	04-81	
D	0238	10-81	
E	0277	12-81	

C8 33pf
RP2-D
C7 33pf
RP2-C
C6 33pf
RP2-B
C5 33pf
RP2-A
C3 33pf
R5 2MΩ
U1 U2
RP1 4 13
RP1 14 3
RP1 16 1
RP1 2 15
RP1 5 12
RP1 11 6
RP1 10 7
RP1 8 9
P1
P̄1
P2
P̄2
TRΦ
AGC
LED
LED
GND
R6 150Ω ½W
R1 200K
R4 82K
VREF (3.0V)
+12V
Q1 2N2222A
R3 4.7K
C9 .1μf
D TST1
1 P1 IN
4 F1
5 F2
E4 "1" 3 M1
E5 "2" 2 M2
C TST2
A P2 IN
7 TST3
E -T ZERO
6 TST4
+12V 9,J +12 VDC
C11 C4 .1μf
11,L,18,19,T,U GND
C10 C2 .1μf
-5V 8,H -5VDC
VREF (3.0V) R2 51Ω 10 VREF
C1 .1μf
G TST6
F TST5

EC HISTORY		MUST CONFORM TO ENGINEERING SPEC. 35000–070		QUANTUM CORPORATION			
DATE	NO.	MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	TITLE SCHEMATIC, XDUCER PCB			
			LINEAR ±.XX / ±.XXX	DETAIL	10-9-80	RELEASED FOR ASSEMBLY	
		CASE DEPTH		DESIGN		20-20010	B
		HARDNESS	ANGULAR±	APPRO		SHEET 1 OF 2	
		SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX / INSIDE MAX	SCALE		80-20010	EC E

BAY REPROGRAPHICS

FIGURE 6-6
TRANSDUCER PCBA SCHEMATIC SHT 1

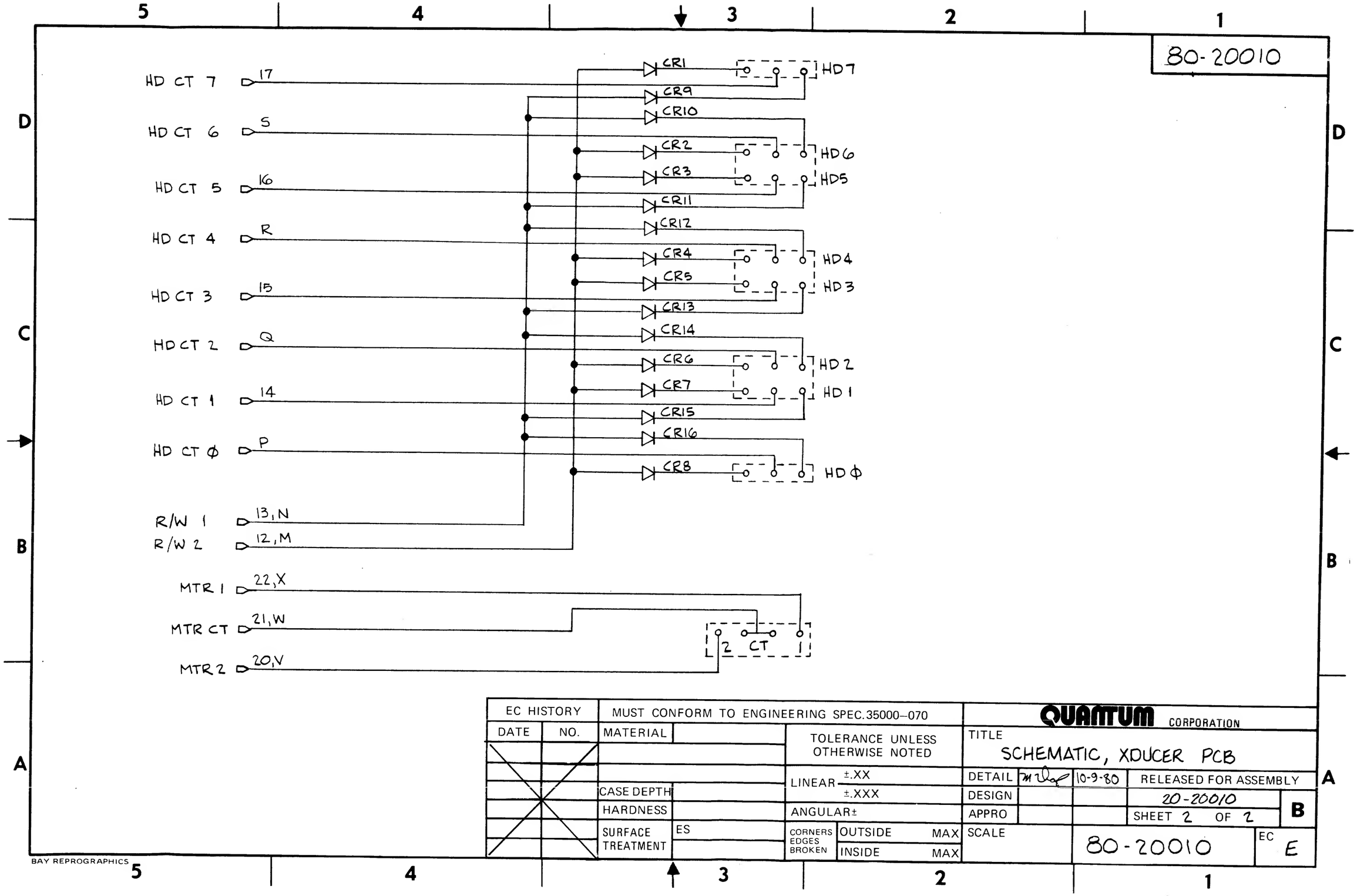
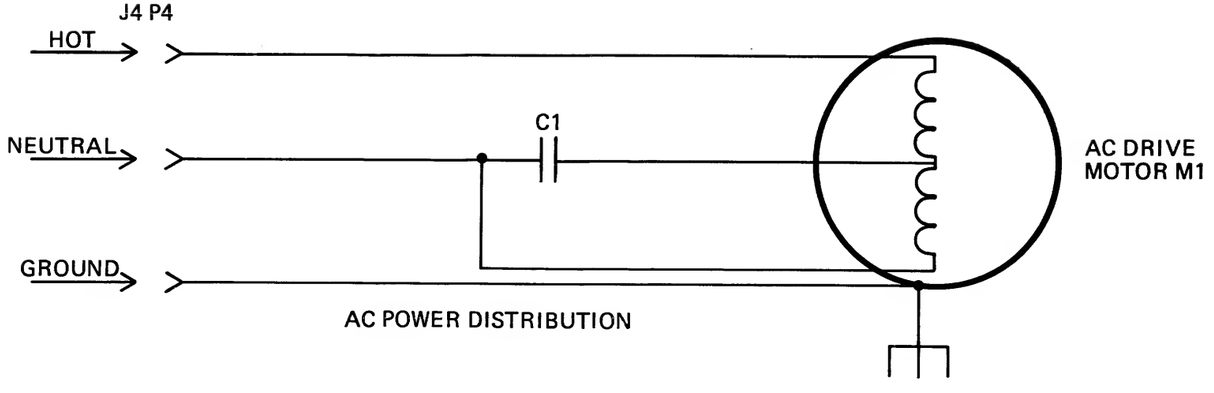


FIGURE 6-7
TRANSDUCER PCBA SCHEMATIC SHT. 2



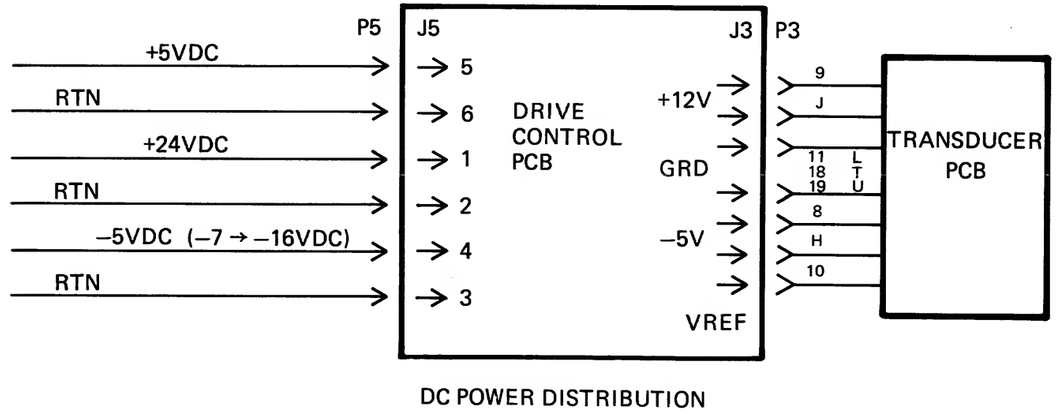


FIGURE 6-8
AC and DC POWER DISTRIBUTION

SECTION 7

ILLUSTRATED PARTS BREAKDOWN

7.1 GENERAL DISCUSSION

This section illustrates the various subassemblies and component parts of the Series 2000. Quantum part numbers are listed by call out numbers on the exploded drawings. Both Quantum and commerical part numbers are given for those electronic parts where appropriate.

7.2 MAJOR ASSEMBLIES

Figure 7-1 is an exploded view of the drive showing

1. Cabinet assembly
2. Drive control PCBA
3. Drive assembly

7.3 SUBASSEMBLIES

Figure 7-2 is an exploded view of the Drive Assembly showing all replacible parts of drive; bubble, head arms, disks, AC Motor Assembly,etc.

Figure 7-3 is an exploded view of the Drive Power Transistor Assembly

Figure 7-4 is an exploded view of the Actuator Sub-Assembly

Figure 7-5 is an exploded view of the Spindle and Disk Sub-Assembly

Figure 7-6 is an exploded view of the Head Arm Sub-Assembly

Figure 7-7 is an exploded view of the Cabinet Sub-Assembly

Figure 7-8 is an exploded view of the AC Drive Motor Assembly

Figure 7-9 is an exploded view of the Bubble Sub-Assembly

7.4 PRINTED CIRCUIT BOARDS

7.4.1 Transducer PCB

Figure 7-10 Shows the component layout of the Transducer PCBA

7.4.2 Drive Control PCB

Figure 7-11 Shows the component layout of the Drive Control PCBA.

Throughout this section notes are used to indicate parts that are not field replaceable, e.g., bottom motor plate, rotor, spindle etc. All under bubble parts are only available to Quantum qualified repair centers.

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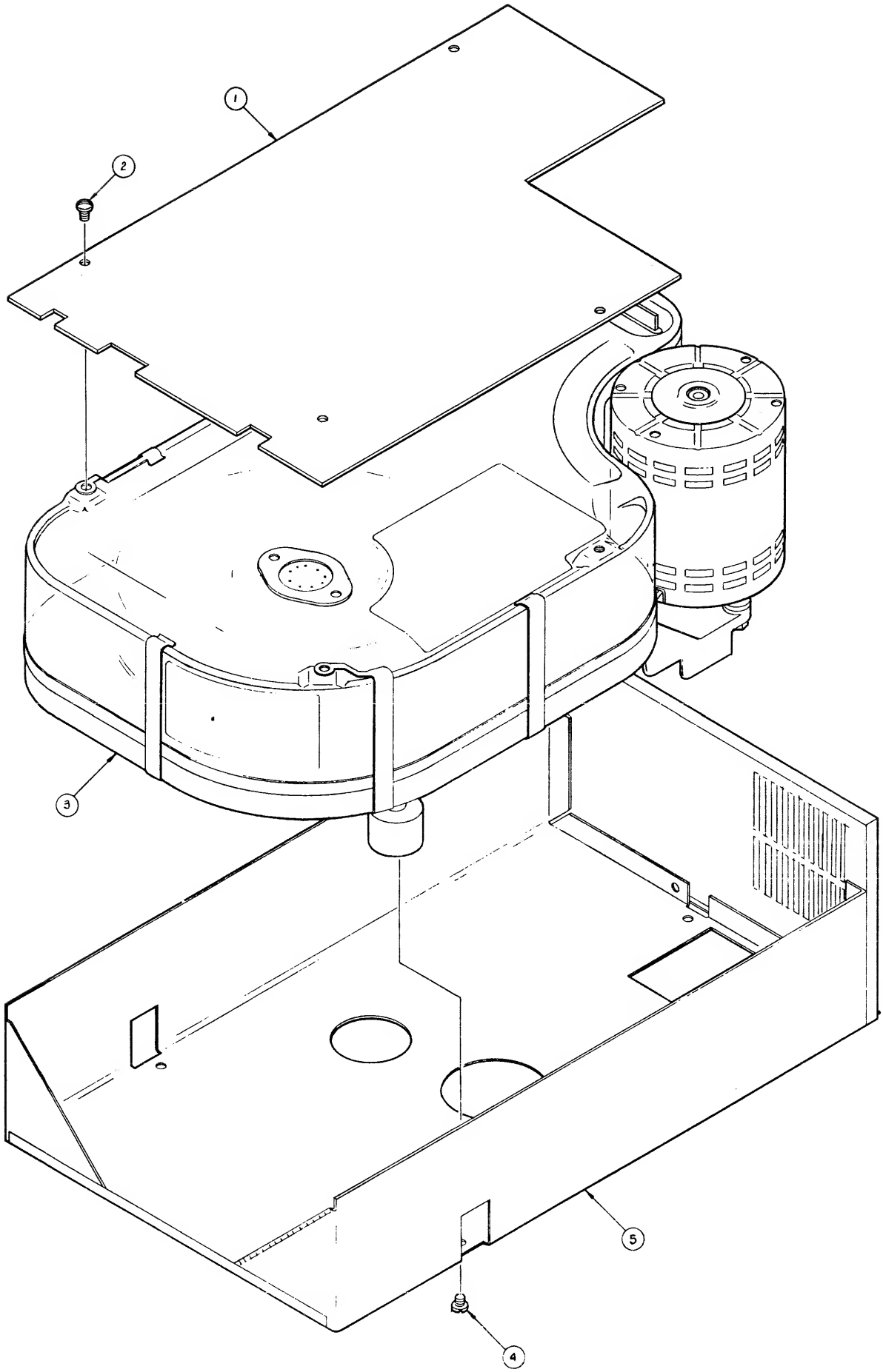

FIGURE 7-1
MAJOR ASSEMBLIES

Series 2000
Major Assemblies

Item	Part Number	Description
1.	20-20000	Drive Control PCBA See figure 7-11.
2.	54-10104	Screw, 8-32 x .38 (4)
3.	NA	Drive Assembly See figure 7-2.
4.	54-10226	Screw, Flat head, 8-32 x .25 (3)
5.	78-40048	Cabinet Sub-Assembly See figure 7-3.

Drive Assembly

Item	Part Number	Description
1.	75-40059	Bubble assembly See figure 7-9
2.	NA	Spindle and Disk assembly See figure 7-5.
3.	38-40003	Filter, Circulation
4.	75-40067	Bracket assm, Power transistor See figure 7-3.
5.	73-40103	Index assembly
6.	36-40129	Mount, shock (3)
7.	58-10299	Ring, retaining
8.	48-40150	Chip, shipping latch
9.	54-1-102	Screw, 8-32 x .25 (2)
10.	43-40044	Strap, capacitor
11.	51-40086	Label, belt guard
12.	75-40130	Belt guard assembly
13.	40-40131	Base, machined
14.		Head arm assembly See figure 7-6.
15.	NA	Actuator sub-assembly See figure 7-4.
16.		AC motor assembly See figure 7-8.
17.	41-40191	Nut, clamp
18.	41-40192	Screw, clamp
19.	54-10102	Screw, 8-32 x .25 (2)
20.	09-40009	Transducer assembly See figure 7-10.
21.	58-10017	O-ring
22.	48-40117	Latch, shipping

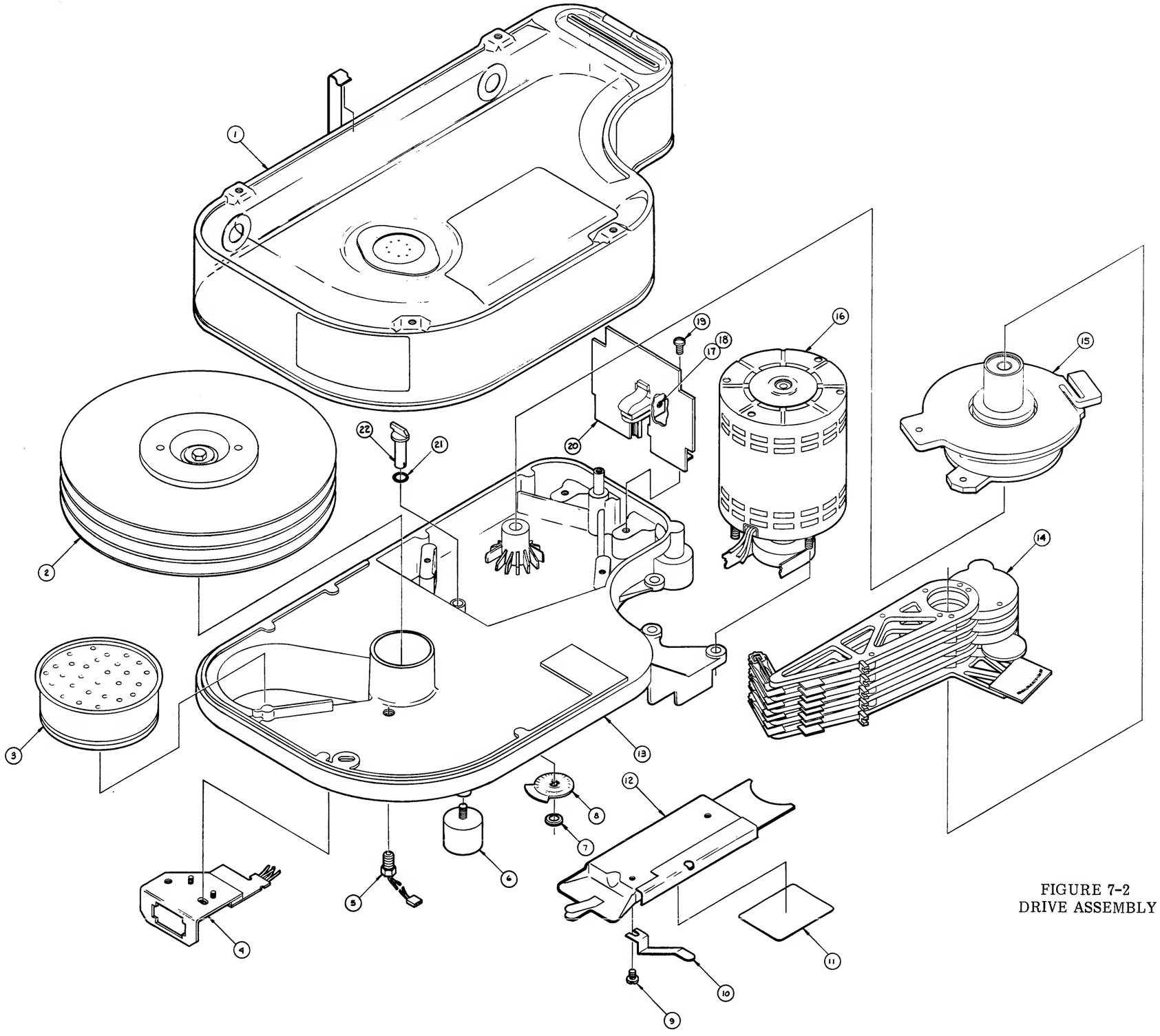

FIGURE 7-2
DRIVE ASSEMBLY

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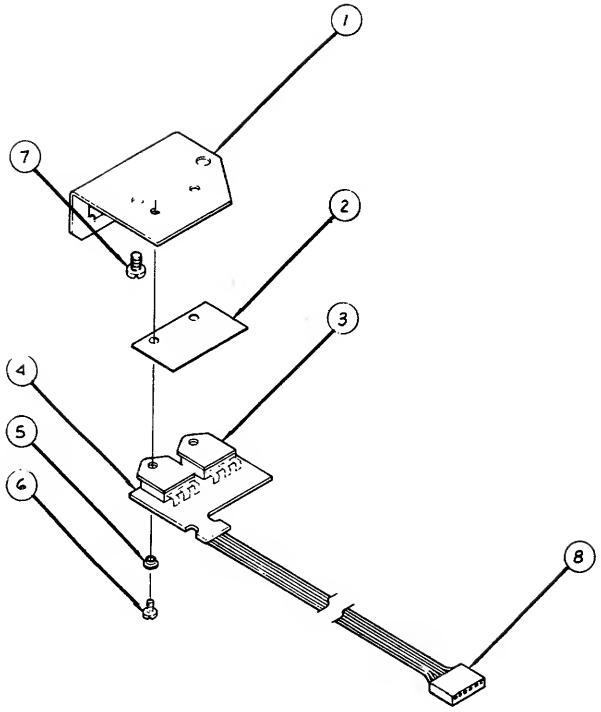

FIGURE 7-3
POWER TRANSISTOR ASSEMBLY

Power Transistor Assembly 75-40067

Item	Part Number	Description
1.	43-40017	Bracket, Connector AC
2.	48-40133	Pad, Transistor Insulating
3.	16-14000	Transistor, TIP 140 Power (2)
4.	10-20040	PCB Transistor
5.	57-10011	Washer, Insulating (2)
6.	54-10143	Screw 4-40 X .25 (2)
7.	54-10102	Screw 8-32 X .25
8.	22-10008	Housing, Connector
	22-10009	Pin, TX Rotor (6)
	31-10054	Wire, 22GA White

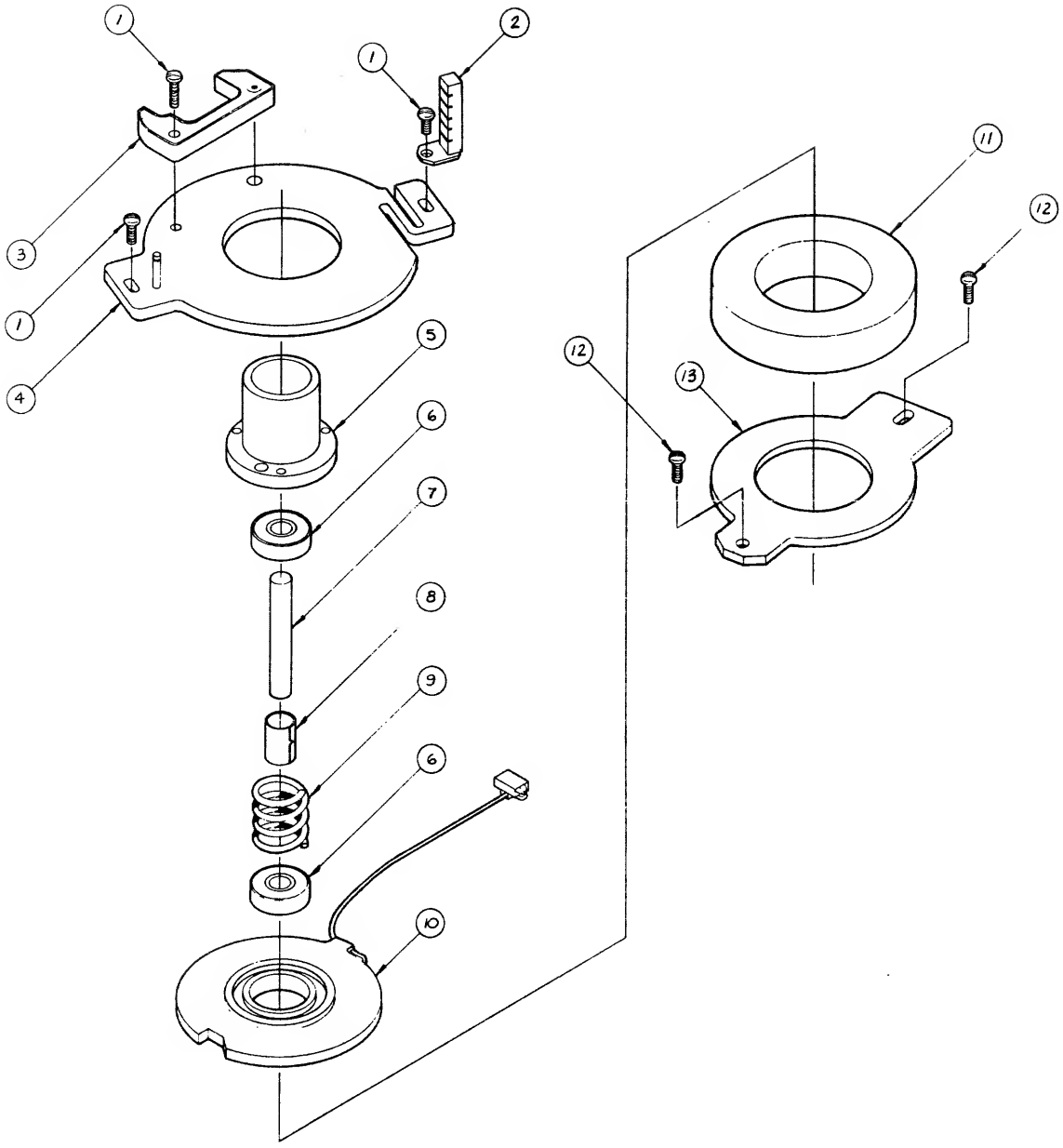

FIGURE 7-4
ACTUATOR SUB-ASSEMBLY

Actuator Sub-Assembly

Item	Part Number	Description
1	54-10106	Screw 8-32 X .50 (2)
2	75-40171	Post Assembly, Pigtail
3	48-40136	Stop, Crash
4	75-40106	Plate Assembly, Upper magnet
5	40-40075	Hub, Actuator See Note 1
6	34-10000	Bearing, Rotor "
7	42-40076	Shaft, Actuator "
8	57-40078	Spacer, Pivot Bearing "
9	33-40077	Spring, Pivot Bearing "
10	75-40196	Rotor/Connector Assembly "
11	24-40062	Magnet Ring See Note 2
12	54-10104	Screw 8-32 X .38 (3)
13	40-40024	Plate, Lower Magnet See Note 2

Note 1...Items 5-10 must be replaced as an assembly. Part number 75-40068 Hub Assembly, Actuator.

Note 2...Items 11,13 must be replaced as an assembly. Part number 75-40105 Plate Assembly, Lower Magnet.

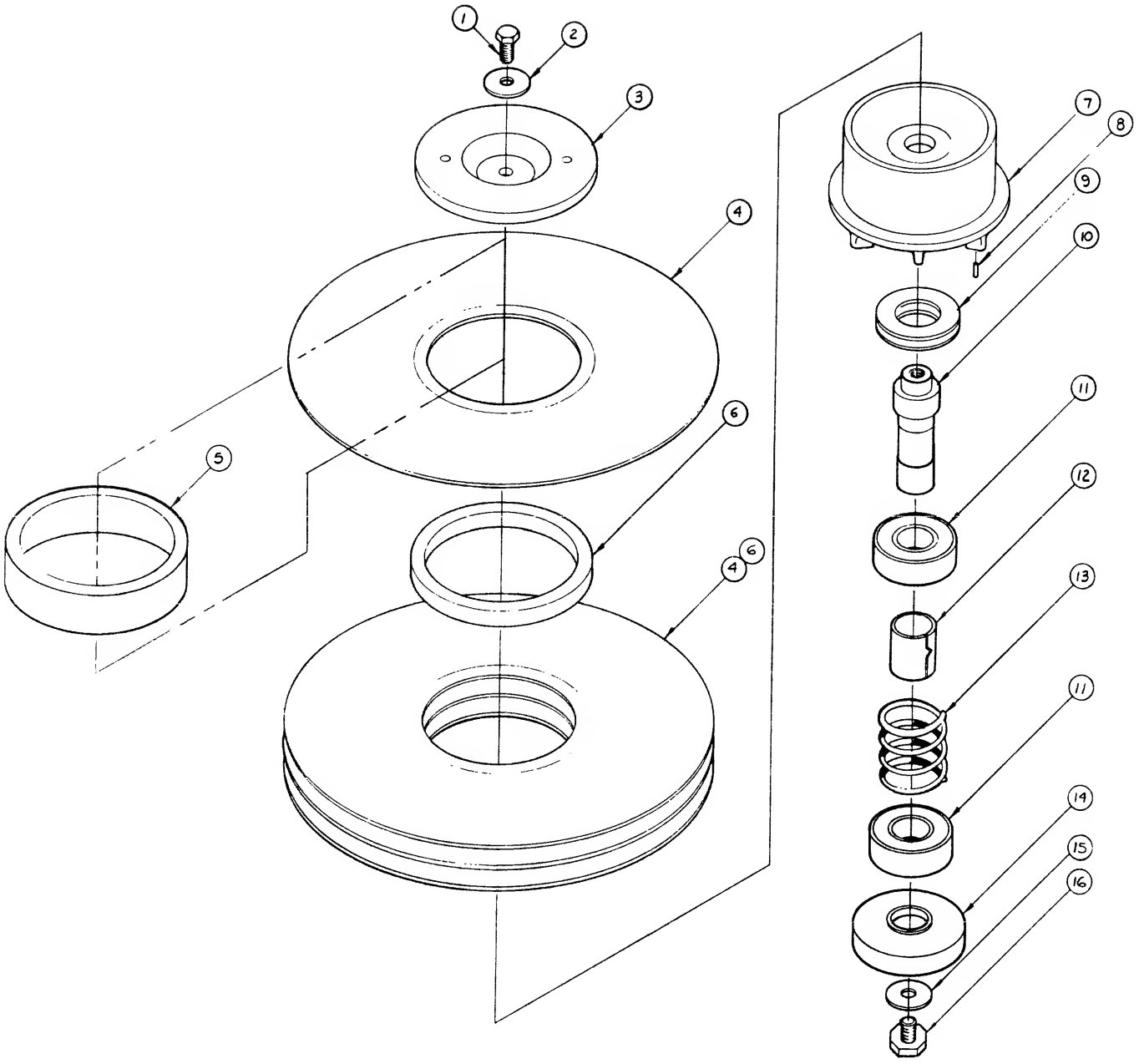

FIGURE 7-5
SPINDLE and DISK SUB ASSEMBLY

Spindle and Disk Sub-assembly

Item	Part Number	Description
1.	54-10213	Screw .25-20 X .62
2.	57-10090	Washer, Spindle Flat
3.	40-40033	Clamp, Disk
4.	61-40204	Disk, 200mm 10MB(1), 20MB(2), 30MB(3), 40MB(4)
5.	40-40028	Spacer, Disk Long 10MB only
	40-40027	Spacer, Disk Mediun 20MB only
	40-40026	Spacer, Disk Short 30MB only
6.	40-40025	Spacer, Disk Common 20MB(1), 30MB(2), 40MB(3)
7.	75-40104	Hub Assembly,Spindle (includes item 8)
8.	57-10012	Pin, Groove
9.	47-40063	Seal, Exculsion
	45-10056	Ferrofluid
	57-40031	Spacer, Spindle Seal
10.	42-40010	Shaft, Spindle See note 1
11.	34-10001	Bearing, Spindle (2) "
12.	57-40037	Spacer,Spindle Bearing "
13.	33-40036	Spring, Spindle Bearing "
14.	40-40038	Pulley, Spindle "
15.	57-10090	Washer, Spindle Flat "
16.	75-40020	Screw Assembly, Ground "

Note 1....Items 10-16 must be replaced as an assembly. Part number 75-40095.

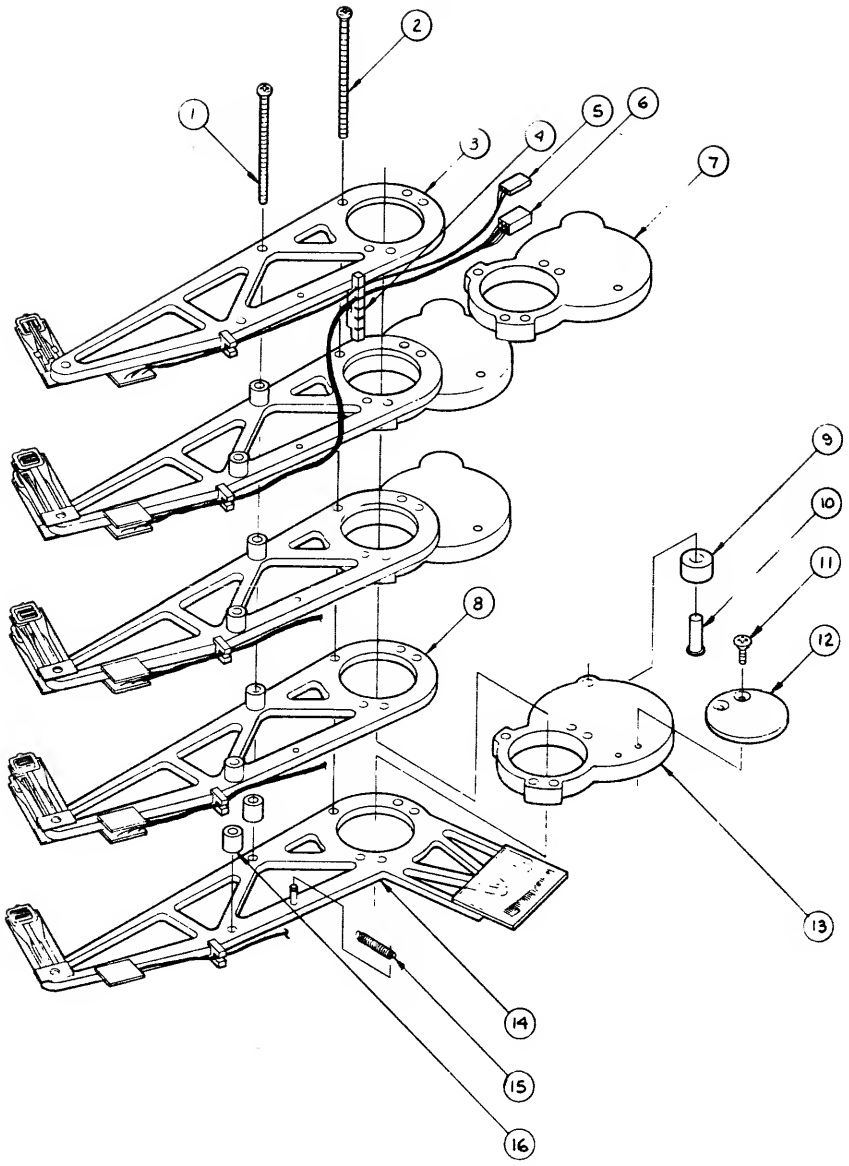

FIGURE 7-6
HEAD ARM SUB-ASSEMBLY

Head Arm Assembly Note 1

Item	Part Number	Description
1.	54-10147	Screw 4-40 X .50 (4) 10MB Arms to arms
	54-10150	Screw 4-40 X .88 (4) 20MB Arms to arms
	54-10153	Screw 4-40 X 1.25 (4) 30MB Arms to arms
	54-10156	Screw 4-40 X 1.62 (4) 40MB Arms to arms
2.	54-10148	Screw 4-40 X .75 (3) 10MB Stack to hub
	54-10151	Screw 4-40 X 1.12 (3) 20MB Stack to hub
	54-10154	Screw 4-40 X 1.50 (3) 30MB Stack to hub
	54-10157	Screw 4-40 X 1.88 (3) 40MB Stack to hub
3.	75-40102	Arm Assembly, Upper
4.	48-40122	Guide, Multicable
5.	22-10040	Housing, Connector (3 pos.)
	22-10043	Pin, Head (3)
6.	22-10041	Housing, Connector Dual (3 pos.)
	22-10043	Pin, Head (6)
7.	40-40090	Counterbalance 20MB(1), 30MB(2), 40MB(3)
8.	75-40108	Arm Assembly, Dual Head 20MB(1), 30MB(2), 40MB(3)
9.	47-40082	Tubing, Stop
10.	58-40084	Pin, Stop
11.	54-10233	Screw 4-40 X .25 (2)
12.	40-40173	Counterweight
13.	40-40141	Counterweight, Main Cast
14.	75-40098	Arm Assembly, Lowest Head
15.	33-40083	Spring, Return
16.	57-40066	Spacer, Head Arm 10MB(2), 20MB(4), 30MB(6), 40MB(8)

Note 1.	75-40100	Head arm assembly, actuator, 10MB
	75-40115	" " " " 20MB
	75-40127	" " " " 30MB
	75-40132	" " " " 40MB

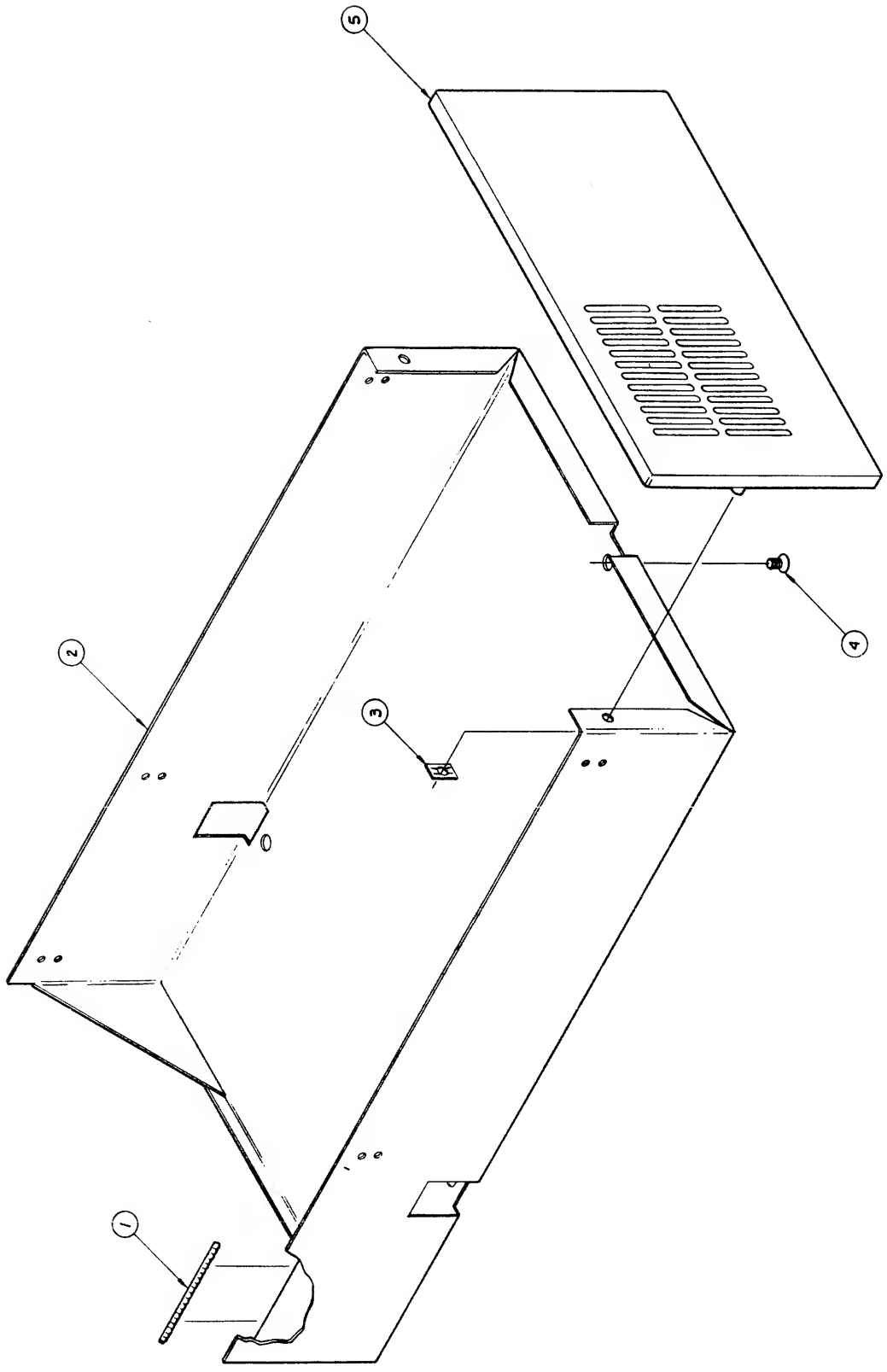

FIGURE 7-7
CABINET SUB-ASSEMBLY

Cabinet Assembly 74-40190

Item	Part Number	Description
1.	48-40177	Grommet, Edge
2.	59-40045	Cabinet
3.	58-10010	Fastener, Push On (3)
4.	54-10226	Screw, Flat Head 8-32 X .25 (3)
5.	48-40047	Plate, Cabinet Face

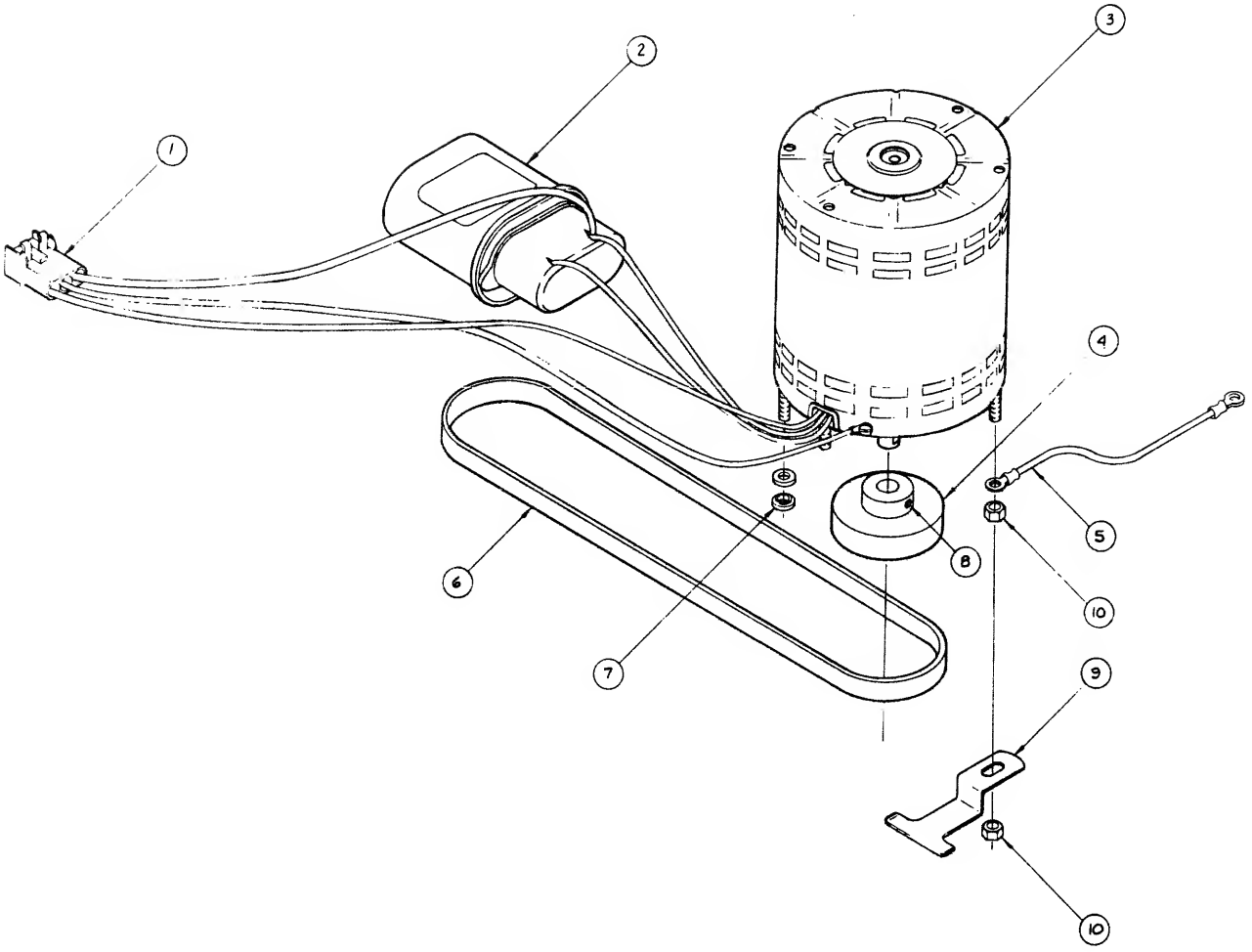

FIGURE 7-8
AC DRIVE MOTOR ASSEMBLY

AC Drive Motor Assembly See note 1

Item	Part Number	Description
1.	22-10003	Housing, AC Connector
	22-10006	Pin, AC Ground
	22-10004	Pin, AC (2)
	31-10050	Wire, 18GA Yellow/Green (AC Ground)
	31-10051	Wire, 18GA White (AC)
2.	03-10088	Capacitor, 110 VAC
	03-10089	Capacitor, 220 VAC
3.	26-40006	Motor, Drive 110 VAC
	26-40007	Motor, Drive 220 VAC
4.	40-40015	Pulley, Motor 60 HZ
	40-40032	Pulley, Motor 50 HZ
5.	74-40180	Strap, AC Motor Ground
6.	50-40000	Belt, Drive 60 HZ
	50-40001	Belt, Drive 50 HZ
7.	57-40039	Washer, Motor Insulating (6)
8.	54-10205	Setscrew, Cup Point 8-32 X .19 (2)
9.	43-40035	Clamp, Pulley Shipping
10.	56-10304	Nut 8-32 X (5)

Note 1 Motor Assembly with pulley, capacitor, and connector for:

110 VAC 60HZ 73-40226
110 VAC 50HZ 73-40227
220 VAC 60HZ 73-40228
220 VAC 50HZ 73-40229

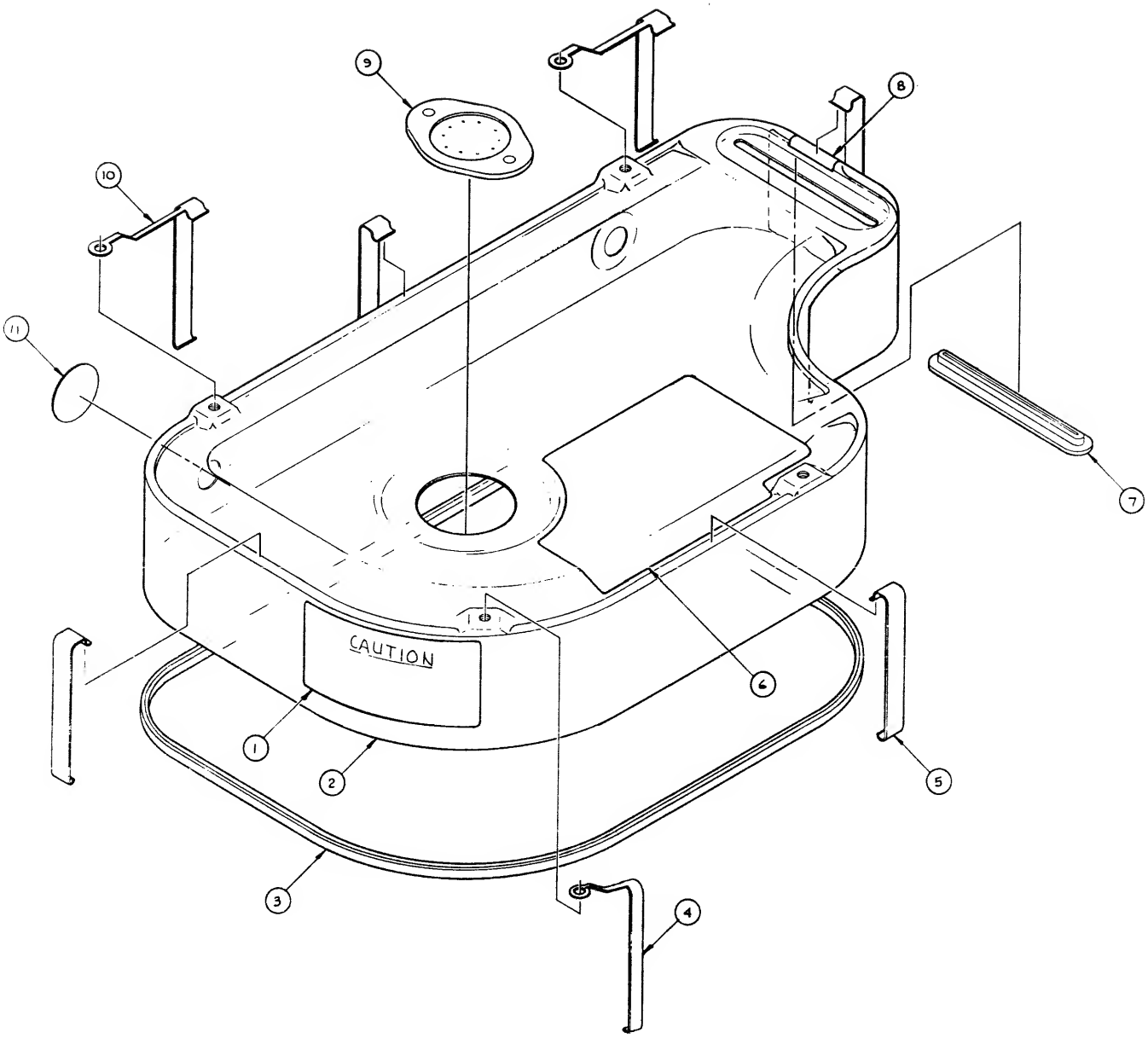

FIGURE 7-9
BUBBLE SUB-ASSEMBLY

Bubble Sub-Assembly

Item	Part Number	Description
1.	51-40087	Label, Chamber
2.	48-40061	Bubble, Plastic
3.	75-40034	Gasket Assembly, Bubble Seal
4.	43-40154	Clamp, Bubble Short ground
5.	43-40058	Clamp, Bubble (4)
6.	51-40183	Label, EMI
7.	46-40046	Seal, Actuator
8.	51-40163	Label, Shield
9.	38-40002	Filter, Breather
10.	43-40155	Clamp, Bubble, Long ground (2)
11.	51-40085	Label, Seal

DRAWING NOT RELEASED

FIGURE 7-10
TRANSDUCER PCBA

Transducer PCB Assembly

Item	Part Number	Description

BILL OF MATERIALS NOT RELEASED AT PUBLICATION

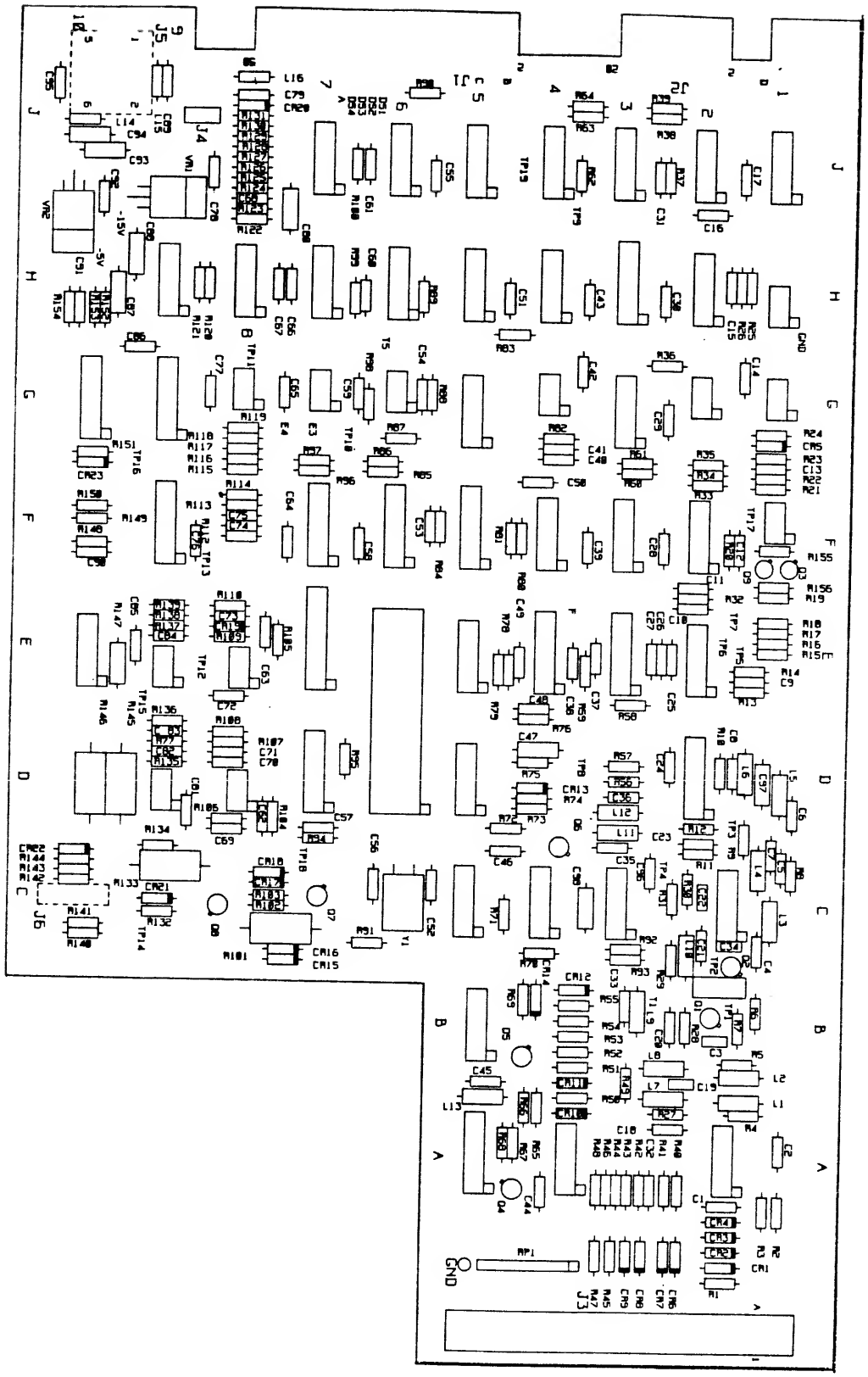

FIGURE 7-11
DRIVE CONTROL PCBA

Drive Control PCB Assembly

RESISTORS

Ref.	Part Number	Description	Ref.	Part Number	Description
R1	01-12215	8.06K 1/8W 1%	R52	01-12209	71.5 1/8W 1%
R2,3	01-12206	5.11K " "	R53	01-12013	3.6K 1/4W 5%
R4	01-12201	249 " "	R54	01-12012	2K " "
R5	01-12202	1K " "	R55	01-12005	330 " "
R6	01-12006	510 1/4W 5%	R56	01-12014	6.8K " "
R7	01-12002	51 " "	R57	01-12012	2K " "
R8	01-12201	249 1/8W 1%	R58	01-12028	240K " "
R9	01-12002	51 1/4W 5%	R59	01-12024	200K " "
R10	01-12012	2K " "	R60	01-12012	2K " "
R11	01-12002	51 " "	R61	01-12018	20K " "
R12,13	01-12012	2K " "	R62	01-12012	2K " "
R14	01-12003	120 " "	R63-65	01-12002	51 " "
R15	01-12012	2K " "	R66	01-12001	20 " "
R16	01-12006	510 " "	R67	01-12005	330 " "
R17	01-12008	1K " "	R68,69	01-12015	5.1K " "
R18	01-12012	2K " "	R70-72	01-12012	2K " "
R19	01-12008	1K " "	R73	01-12018	20K " "
R20	01-12012	2K " "	R74	01-12012	2K " "
R21	01-12005	330 " "	R75	01-12016	10K " "
R22	01-12004	220 " "	R76	01-12020	36K " "
R23	01-12026	1M " "	R77	01-12022	56K " "
R24,25	01-12016	10K " "	R78	01-12018	20K " "
R26	01-12050	160K " "	R79	01-12012	2K " "
R27	01-12201	249 1/8W 1%	R80	01-12204	2.49K 1/8W 1%
R28	01-12002	51 1/4W 5%	R81	01-12203	1.69K " "
R29	01-12006	510 " "	R82	01-12206	5.11K " "
R30	01-12003	120 " "	R83	01-12012	2K 1/4W 5%
R31	01-12201	249 1/8W 1%	R84	01-12202	1K 1/8W 1%
R32	01-12003	120 1/4W 5%	R85,86	01-12012	2K 1/4W 5%
R33,34	01-12012	2K " "	R87,88	01-12016	10K " "
R35	01-12018	20K " "	R89	01-12012	2K " "
R36,37	01-12012	2K " "	R90	01-12004	220 " "
R38,39	01-12002	51 " "	R91	01-12012	2K " "
R40,41	01-12207	1.50K 1/8W 1%	R92,93	01-12003	120 " "
R42	01-12018	20K 1/4W 5%	R94,95	01-12207	1.50K 1/8W 1%
R43	01-12006	510 " "	R96,97	01-12012	2K 1/4W 5%
R44	01-12015	5.1K " "	R98	01-12016	10K " "
R45	01-12018	20K " "	R99	01-12015	5.1K " "
R46	01-12015	5.1K " "	R100	01-12005	330 " "
R47	01-12018	20K " "	R101	01-12301	2 3W "
R48	01-12006	510 " "	R102	01-12012	2K 1/4W "
R49	01-12008	1K " "	R103	01-12006	510 " "
R50	01-12012	2K " "	R104	01-12013	3.6K " "
R51	01-12008	1K " "	R105	01-12003	120 " "

Drive Control PCB Assembly (cont'd)

Ref.	Part Number	Description	Ref.	Part Number	Description
R106	01-12008	1K " "	R128	01-12006	510 1/4W 5%
R107,8	01-12022	56K " "	R129,30	01-12015	5.K " "
R109	01-12205	4.02K 1/8W 1%	R131	01-12012	2K " "
R110	01-12012	2K 1/4W 5%	R132	01-12004	220 " "
R111	NOT USED		R133	01-12300	1 2W "
R112,13	01-12002	51 " "	R134	01-12012	2K 1/4W "
R114	01-12012	2K " "	R135	01-12022	56K " "
R115	01-12024	200K " "	R136	01-12010	1.3K " "
R116	01-12015	5.1K " "	R137	01-12020	36K " "
R117	01-12012	2K " "	R138,39	01-12017	18K " "
R118	01-12024	200K " "	R140	01-12004	220 " "
R119	01-12015	5.1K " "	R141,42	01-12013	3.6K " "
R120	01-12013	3.6K " "	R143,44	01-12004	220 " "
R121	01-12008	1K " "	R145,46	01-12300	1 2W "
R122,23	01-12012	2K " "	R147	01-12304	300 1/2W "
R124	01-12024	200K " "	R148-50	01-12012	2K 1/4W "
R125,26	01-12015	5.1K " "	R151-54	01-12016	10K " "
R127	01-12016	10K " "			
6J	02-12302	220/330 14pin DIP	RP1	02-12303	22K 10pin SIP

CAPICATORS

C1	03-16102	.1uf ±10% C 50V	C34	03-16208	39pf ±5% M CM05
C2	03-16200	.1uf +80-20% 50V	C35,36	03-16200	.1uf +80-20% 50V
C3	03-16203	180pf ±10% C 50V	C37	03-16103	1000pf ±10% C 50V
C4	03-16100	.01uf ±10% C 50V	C38,39	03-16200	.1uf +80-20% 50V
C5-7	03-16200	.1uf +80-20% 50V	C40	03-16003	100pf ±10% C 50V
C8	03-1620	.01uf ±10% C 50V	C41	03-16000	22pf ±10% C 50V
C9,10	03-16003	100pf ±10% C 50V	C42-46	03-16200	.1uf +80-20% 50V
C11	03-16103	1000pf ±10% C 50V	C47	03-16201	4.7uf ± 10% 35V
C12	03-16200	.1uf +80-20% 50V	C48	03-16101	.033uf ±10% C 50V
C13	03-16102	.1uf ±10% C 50V	C49	03-16103	1000pf ±10% C 50V
C14	03-16200	.1uf +80-20% 50V	C50,51	03-16200	.1uf +80-20% 50V
C15	03-16100	.01uf ±10% C 50V	C52	03-16000	22pf ±10% C 50V
C16-18	03-16200	.1uf +80-20% 50V	C53	03-16005	510pf ±10% C 50V
C19	03-16202	62pf ±5% M CMO5	C54,55	03-16200	.1uf +80-20% 50V
C20	03-16200	.1uf +80-20% 50V	C56,57	03-16000	22pf ±10% C 50V
C21	03-16100	.01uf ±10% C 50V	C58-61	03-16200	.1uf +80-20% 50V
C22	03-16203	180pf ±5% M CMO5	C62	03-16101	.033uf ±10% C 50V
C23	03-16100	.01uf ±10% C 50V	C63-67	03-16200	.1uf +80-20% 50V
C24	03-16000	22pf ±10% C 50V	C68	03-16100	.01uf ±10% C 50V
C25-27	03-16102	.1uf ±10% C 50V	C69,70	03-16200	.1uf +80-20% 50V
C28	03-16200	.1uf +80-20% 50V	C71	03-16003	100pf ±10% C 50V
C23	03-16100	.01uf ±10% C 50V	C72	03-16100	.01uf ±10% C 50V

Drive Control PCB Assembly (cont'd)

Ref.	Part Number	Description	Ref.	Part Number	Description
C73	03-16200	.1uf +80-20% 50V	C84	03-16003	1000pf ±10% C 50V
C74,75	03-16102	.1uf ±10% C 50V	C85,86	03-16200	.1uf +80-20% 50V
C76,77	03-16200	.1uf +80-20% 50V	C87,88	03-16201	4.7uf ±10% 35V
C78	03-16100	.01uf ±10% C 50V	C89-92	03-16200	.1uf +80-20% 50V
C79	03-16200	.1uf +80-20% 50V	C93,94	03-16201	4.7uf ±10% 35V
C78	03-16100	.01uf ±10% C 50V	C95,96	03-16200	.1uf +80-20% 50V
C80	03-16201	4.7uf ±10% 35V	C97,98	03-16201	4.7uf ±10% 35V
C81	03-16200	.1uf +80-20% 50V	C99	03-16102	.1uf ±10% C 50V
C82	03-16003	100pf ±10% C 50V			
C83	03-16101	.033uf ±10% C 50V			

"C" indicates CERAMIC part. "M" indicates MICA part

INDUCTORS

L1	04-16501	2.7 uh shielded	L8	04-16502	12 uh shielded
L2	04-16502	12 uh "	L9	04-16504	150 uh "
L3	04-16507	15 uh "	L10	04-16507	15 uh "
L4,5	04-16500	2.2 uh unshielded	L11	04-16503	18 uh "
L6	04-16503	18 uh shielded	L12,13	04-16500	2.2 uh unshielded
L7	04-16501	2.7.uh "	L14-16	04-16506	Ferrite bead

TRANSISTORS

Q1-3	16-14001	Transistor, 2N2222
Q4	16-14002	Transistor, 2N2907
Q5-7	16-14001	Transistor, 2N2222
Q8	16-14002	Transistor, 2N2907

DIODES

CR1-10	16-14003	Diode, 1N4148	CR17	16-14003	Diode, 1N4148
CR11	16-14005	Zener, 3V, 1N5525B	CR18-19	16-14005	Zener, 3V 1N5525B
CR12	16-14003	Diode, 1N4148	CR20-22	16-14003	Diode, 1N4148
CR13-14	16-14005	Zener, 3V ,1N5525B	CR23	16-14006	Zener, 5.1V. 1N5231B
CR15-16	16-14004	Diode, 1N4003			

INTERGRATED CIRCUITS

Ref.	Part Number	Description	Ref.	Part Number	Description
1A,1C	13-18204	NE592	5C	13-18004	7407
1F	13-18211	LM311P	5D	13-18009	7474 (LS)
1G	13-18209	LF13741	5E	13-18002	7404
1H	13-18202	LF398N	5F	13-18208	MC1408L8
2D	13-18205	8T20	5G	13-18034	74107A (LS)
2E	13-18011	7486 (LS)	5H	13-18005	7408 (LS)
2F	13-18007	7438	5J	13-18007	7438
2G	13-18202	LF398N	6F	13-18019	74257 (LS)
2H	13-18001	7402 (LS)	6G	13-18209	LF13741
2J	13-18206	75110	6H	13-18009	7474 (LS)
3C	13-18204	NE592	7D	13-18208	MC1408L8
3E	13-18016	74123 (LS)	7E	13-18013	74374 (LS)
3F	13-18000	7400 (LS)	7F	13-18019	74257 (LS)
3G	13-18212	LM1414	7G	13-18211	LM311P
3H	13-18014	74390 (LS)	7H	13-18001	7402 (LS)
3J	13-18207	75107	7J	13-18006	7414
4A	13-18203	Q2T2907	8D	13-18209	LF13741
4C	13-18009	7474 (LS)	8G	13-18211	LM311P
4E	13-18016	74123 (LS)	8H	13-18213	74374 (LS)
4F	13-18015	74393 (LS)	9D,9E	13-18209	LF13741
4G	13-18214	LM 301	9F	13-18018	74175 (LS)
4H	13-18002	7404	9G	13-18010	7475 (LS)
4J	13-18000	7400 (LS)	9H	13-18011	7486 (LS)
5A	13-18008	7445	10E	13-18003	7406
5B	13-18003	7406	10G	13-18210	LF13509
VR1	13-18217	78M12C, +12v reg	VR2	13-18216	79M05C, -5v reg

MISCELLANEOUS

Y1	11-10086	Crystal, 6MHZ	J5	22-10032	Connector, DC PWR
6J	22-10085	Socket, 14 pin	J6	22-10038	Header, Index
6D	22-10079	Socket, 40 pin	Test Pt	22-10035	
J3	22-10034	Connector, bubble	Plug St	22-10036	
J4	22-10033	Header, Index	Screw	54-10111	4-40 x .25 (2)
Nut	56-10322	4-40 Kept			