## Description

The µPD765A/B is an LSI floppy disk controller (FDC) chip which contains the circuitry and control functions for interfacing a processor to 4 floppy disk drives. It is capable of either IBM 3740 single density format (FM), or IBM System 34 double density format (MFM) including double-sided recording. The µPD765A/B provides control signals which simplify the design of an external phase-locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy disk interface.

Hand-shaking signals are provided in the µPD765A/B which make DMA operation easy to incorporate with the aid of an external DMA controller chip, such as the µPD8257. The FDC will operate in either the DMA or non-DMA mode. In the non-DMA mode the FDC generates interrupts to the processor every time a data byte is to be transferred. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC and DMA controllers.

There are 16 commands which the µPD765A/µPD765B will execute. Most of these commands require multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available.

| | |
|---|---|
| Read Data | Read Deleted Data |
| Read ID | Write Data |
| Specify | Write ID (Format Write) |
| Read Diagnostic | Write Deleted Data |
| Scan Equal | Seek |
| Scan High or Equal | Recalibrate |
| Scan Low or Equal | Sense Interrupt Status |
| Version | Sense Drive Status. |

## Ordering Information

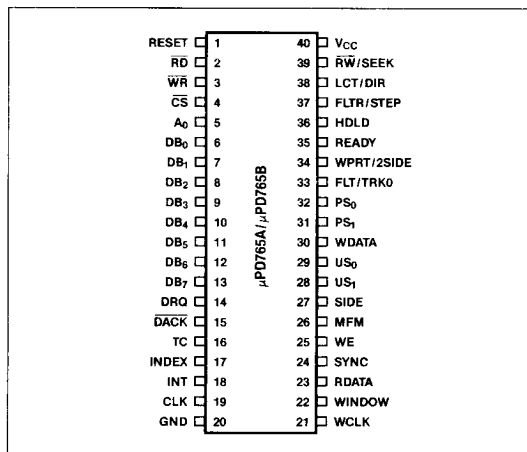| Device Number | Package Type | Max Freq. of Operation |
|---|---|---|
| µPD765AC2 | 40-pin plastic DIP | 8 MHz |
| µPD765B | 40-pin plastic DIP | 8 MHz |

## Features

Address mark detection circuitry is internal to the FDC which simplifies the phase-locked loop and read electronics. The track stepping rate, head load time, and head unload time are user-programmable. The µPD765A/µPD765B offers additional features such as multi-track and multi-side read and write commands and single and double density capabilities.

☐ FM, MFM Control

☐ Variable recording length: 128, 256, . . . 8192 bytes/ sector

☐ IBM-compatible format (single- and double-sided, single- and double-density)

☐ Multi-sector and multi-track transfer capability

☐ Drive up to 4 floppy or micro floppydisk drives

☐ Data scan capability — will scan a single sector or an entire cylinder comparing byte-for-byte host memory and disk data

☐ Data transfers in DMA or non-DMA mode

☐ Parallel seek operations on up to four drives

☐ Compatible with µPD8080/85, µPD8086/88, V-series and µPD780 (Z80®) microprocessors

☐ Single-phase clock: 8 MHz maximum

☐ +5 V only

* Z80 is a registered trademark of the Zilog Corporation.

## Pin Configuration



| | | | |
|---|---|---|---|
| RESET | 1 | 40 | $V_{CC}$ |
| $\overline{RD}$ | 2 | 39 | $\overline{RW}$/SEEK |
| $\overline{WR}$ | 3 | 38 | LCT/DIR |
| $\overline{CS}$ | 4 | 37 | FLTR/STEP |
| $A_0$ | 5 | 36 | HDLD |
| $DB_0$ | 6 | 35 | READY |
| $DB_1$ | 7 | 34 | WPRT/2SIDE |
| $DB_2$ | 8 | 33 | FLT/TRK0 |
| $DB_3$ | 9 | 32 | $PS_0$ |
| $DB_4$ | 10 | 31 | $PS_1$ |
| $DB_5$ | 11 | 30 | WDATA |
| $DB_6$ | 12 | 29 | $US_0$ |
| $DB_7$ | 13 | 28 | $US_1$ |
| DRQ | 14 | 27 | SIDE |
| $\overline{DACK}$ | 15 | 26 | MFM |
| TC | 16 | 25 | WE |
| INDEX | 17 | 24 | SYNC |
| INT | 18 | 23 | RDATA |
| CLK | 19 | 22 | WINDOW |
| GND | 20 | 21 | WCLK |

µPD765A/µPD765B

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## Pin Identification

| No. | Symbol | Function |
|---|---|---|
| 1 | RESET | Reset input |
| 2 | $\overline{RD}$ | Read control input |
| 3 | $\overline{WR}$ | Write control input |
| 4 | $\overline{CS}$ | Chip select input |
| 5 | $A_0$ | Data or status select input |
| 6–13 | $DB_0$–$DB_7$ | Bidirectional data bus |
| 14 | DRQ | DMA request output |
| 15 | $\overline{DACK}$ | DMA acknowledge input |
| 16 | TC | Terminal count input |
| 17 | INDEX | Index input |
| 18 | INT | Interrupt request output |
| 19 | CLK | Clock input |
| 20 | GND | Ground |
| 21 | WCLK | Write clock input |
| 22 | WINDOW | Read data window input |
| 23 | RDATA | Read data input |
| 24 | SYNC | VCO sync output |
| 25 | WE | Write enable output |
| 26 | MFM | MFM output |
| 27 | SIDE | Head select output |
| 28, 29 | $US_0$, $US_1$ | FDD unit select output |
| 30 | WDATA | Write data output |
| 31, 32 | $PS_0$, $PS_1$ | Preshift output |
| 33 | FLT / TRK0 | Fault / track zero input |
| 34 | WPRT / 2SIDE | Write protect / two side input |
| 35 | READY | Ready input |
| 36 | HDLD | Head load output |
| 37 | FLTR / STEP | Fault reset / step output |
| 38 | LCT / DIR | Low current direction output |
| 39 | $\overline{RW}$ / SEEK | Read / write / seek output |
| 40 | $V_{CC}$ | DC power ( +5 V) |

## Pin Functions

### RESET (Reset)

The RESET input places the FDC in the idle state. It resets the output lines to the FDD to 0 (low), except PS0, 1 and WDATA (undefined), INT and DRQ also go low; DB0–7 goes to an input state. It does not affect SRT, HUT, or HLT in the Specify command. If the RDY input is held high during reset, the FDC will generate an interrupt within 1.024 ms. To clear this interrupt, use the Sense Interrupt Status command.

### $\overline{RD}$ (Read Strobe)

The RD input allows the transfer of data from the FDC to the data bus when low and either $\overline{CS}$ or $\overline{DACK}$ is asserted.

### $\overline{WR}$ (Write Strobe)

The $\overline{WR}$ input allows the transfer of data to the FDC from the data bus when low. Disabled when $\overline{CS}$ is high.

### $A_0$ (Data / Status Select)

The $A_0$ input selects the data register ($A_0 = 1$) or status register ($A_0 = 0$) contents to be accessed through the data bus.

### $\overline{CS}$ (Chip Select)

The FDC is selected when $\overline{CS}$ is low, enabling $\overline{RD}$ and $\overline{WR}$.

### $DB_0$–$DB_7$ (Data Bus)

$DB_0$–$DB_7$ are a bidirectional 8-bit data bus. Disabled when $\overline{CS}$ is high.

### DRQ (DMA Request)

The FDC asserts the DRQ output high to request a DMA transfer.

### $\overline{DACK}$ (DMA Acknowledge)

When the $\overline{DACK}$ input is low, a DMA cycle is active and the controller is performing a DMA transfer.

### TC (Terminal Count)

When the TC input is high, it indicates the termination of a DMA transfer. It terminates data transfer during Read/Write/Scan commands in DMA or interrupt mode.

### INDEX (Index)

The INDEX input goes high at the beginning of a disk track.

### INT (Interrupt)

The INT output is FDC's interrupt request. In Non-DMA mode, the signal is output for each byte. In DMA mode, it is output at the termination of a command operation.

### CLK (Clock)

CLK is the input for the FDC's single-phase, TTL-level squarewave clock: 8 MHz or 4 MHz. (Requires a pull-up resistor.)

## WCLK (Write Clock)

The WCLK input sets the data write rate to the FDD. It is 500 kHz for FM, 1 MHz for MFM drives, for 8 MHz operation of the FDC; 250 kHz FM or 500 kHz MFM for 4 MHz FDC operation.

This signal must be input for read and write cycles. WCLK's rising edge must be synchronized with CLK's rising edge, except for the μPD765B.

## WINDOW (Read Data Window)

The WINDOW input is generated by the phase-locked loop (PLL). It is used to sample data from the FDD and in distinguishing between clock and data bits in the FDC.

## RDATA (Read Data)

The RDATA input is the read data from the FDD, containing clock and data bits. To avoid a deadlock situation, input RDATA and WINDOW together.

## WDATA (Write Data)

WDATA is the serial clock and data output to the FDD.

## WE (Write Enable)

The WE output enables write data into the FDD.

## SYNC (VCO Sync)

The SYNC output inhibits the VCO in the PLL when low, enables it when high.

## MFM (MFM Mode)

The MFM output shows the VCO's operation mode. It is high for MFM, low for FM.

## SIDE (Head Select)

Head 1 is selected when the SIDE output is 1 (high), head 0 is selected when SIDE is 0 (low).

## US$_0$, US$_1$ (Unit Select 0, 1)

The US$_0$ and US$_1$ outputs select up to 4 floppy disk drive units using an external decoder.

## PS$_0$, PS$_1$ (Preshift 0, 1)

The PS$_0$ and PS$_1$ outputs are the write precompensation request signals for MFM mode. They determine early, late, and normal times for WDATA shifting.

| PS0 | PS1 | Shift (MFM WDATA) |
|---|---|---|
| 0 | 0 | Normal |
| 0 | 1 | Late |
| 1 | 0 | Early |
| 1 | 1 | — |

## READY (Ready)

The READY input indicates that the FDD is ready to receive data.

## HDLD (Head Load)

The HDLD output is the command which causes the read/write head in the FDD to contact the diskette.

## FLT/TRK0 (Fault/Track 0)

In the read/write mode, the FLT input detects FDD fault conditions. In the seek mode, TRK0 indicates track 0 head position.

## WPRT/2SIDE (Write Protect/Two Side)

In the read/write mode, the WPRT input senses write protected status (at the drive or media.) In the seek mode, 2SIDE senses two-sided media.

## FLTR/STEP (Fault Reset/Step)

In the read/write mode, the FLTR output resets the fault flip-flop in the FDD. In the seek mode, STEP outputs step pulses to move the head to another cylinder. A fault reset pulse is issued at the beginning or each Read or Write command prior to the HDLD signal.

## LCT/DIR (Low Current/Direction)

In the read/write mode, the LCT output indicates that the R/W head is positioned at cylinder 42 or greater. In the seek mode, the DIR output determines the direction the head will move in when it receives a step pulse. If DIR is 0, seeks are performed in the outward direction; DIR is 1, seeks are performed in the inward direction.

## RW/SEEK (Read/Write/Seek)

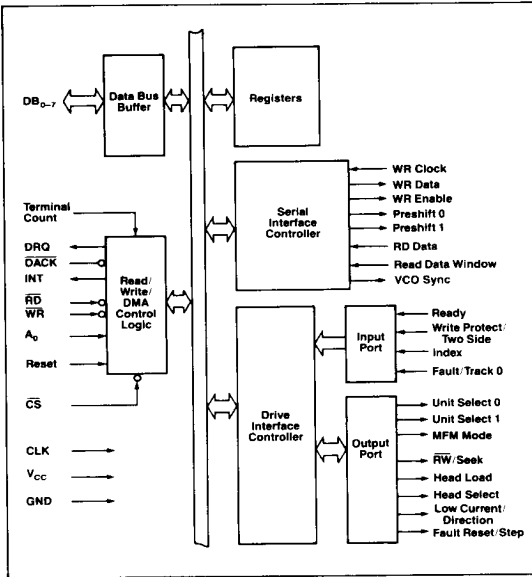The RW/SEEK output specifies the read/write mode when low, and the seek mode when high.

## GND (Ground)

Ground.

## V$_{CC}$ (+5 V)

+5 V power supply.

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## Block Diagram



## Absolute Maximum Ratings

$T_A = 25°C$

| | |
|---|---|
| Power supply voltage, $V_{CC}$ | $-0.5$ to $+7$ V |
| Input voltage, $V_I$ | $-0.5$ to $+7$ V |
| Output voltage, $V_O$ | $-0.5$ to $+7$ V |
| Operating temperature, $T_{OPT}$ | $-10°C$ to $+70°C$ |
| Storage temperature, $T_{STG}$ | $-65°C$ to $+150°C$ |

**Comment:** Exposing the device to stresses above those listed in the Absolute Maximum Ratings could cause permanent damage. The device should not be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5 V \pm 10\%$

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Input voltage low | $V_{IL}$ | $-0.5$ | | $+0.8$ | V | |
| Input voltage high | $V_{IH}$ | 2.0 | | $V_{CC}+0.5$ | V | |
| Output voltage low | $V_{OL}$ | | | 0.45 | V | $I_{OL} = 2.0\,mA$ |
| Output voltage high | $V_{OH}$ | 2.4 | | $V_{CC}$ | V | $I_{OH} = -200\,\mu A$ |
| Input voltage low (CLK + WCLK) | $V_{IL}(\Phi)$ | $-0.5$ | | 0.65 | V | |
| Input voltage high (CLK + WCLK) | $V_{IH}(\Phi)$ | 2.4 | | $V_{CC}+0.5$ | V | |
| Supply current ($V_{CC}$) | $I_{CC}$ | | | 150 | mA | μPD765AC2 |
| | | | | 140 | mA | μPD765B |
| Input load current high | $I_{LIH}$ | | | 10 | $\mu A$ | $V_{IN} = V_{CC}$ |
| Input load current low | $I_{LIL}$ | | | $-10$ | $\mu A$ | $V_{IN} = 0\,V$ |
| Output leakage current high | $I_{LOH}$ | | | 10 | $\mu A$ | $V_{OUT} = V_{CC}$ |
| Output leakage current low | $I_{LOL}$ | | | $-10$ | $\mu A$ | $V_{OUT} = +0.45\,V$ |

## Capacitance

$T_A = 25°C$, $f_C = 1\,MHz$, $V_{CC} = 0\,V$

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Input clock capacitance | $C_{IN}(\Phi)$ | | | 20 | pF | (Note 1) |
| Input capacitance | $C_{IN}$ | | | 10 | pF | (Note 1) |
| Output capacitance | $C_{OUT}$ | | | 20 | pF | (Note 1) |

**Note:**
(1) All pins except pin under test tied to AC ground.

## DIFFERENCES BETWEEN μPD765A AND μPD765B

The μPD765B is a functionally enhanced version of the μPD765A. Differences are explained below.

### Overrun Bit [OR]

In μPD765A, when executing a read- or write-type command (except READ ID and SCAN types), the result status OR bit is not set if there is an overrun on the final byte of a sector. An improvement in the μPD765B allows it to set the OR bit in any situation.

### DRQ Reset

When an overrun occurs, the μPD765A needs $\overline{DACK}$ input to reset DRQ. If $\overline{DACK}$ is not available, an external DMA controller continues to operate even after the FDC enters the R-Phase (Result Phase), and stored result status may be transferred accidentally as ordinary data.

On the other hand, the μPD765B resets DRQ automatically just before the R-Phase entry and independent of the $\overline{DACK}$ input. See AC Characteristics for DRQ reset timing.

### Clock Synchronization

The μPD765B does not require synchronization between the CLK and WCLK inputs.

### Version Command

The Version command distinguishes the μPD765B from other devices. The ST0 response to the Version command is:

| Part No. | ST0 Value |
| --- | --- |
| μPD765A | 80H |
| μPD765B | 90H |

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## AC Characteristics

$T_A = -10$ to $+70°C$; $V_{CC} = +5\ V \pm10\%$

| Parameter | Symbol | Min | Typ (1) | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Clock period | $\Phi_{CY}$ | 120 | 125 | 500 | ns | 8-MHz CLK |
| | | 240 | 250 | 500 | ns | 4-MHz CLK |
| Clock active (high, low) | $\Phi_0$ | 40 | | | ns | |
| Clock rise time | $\Phi_R$ | | | 20 | ns | |
| Clock fall time | $\Phi_F$ | | | 20 | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{RD}\downarrow$ | $t_{AR}$ | 0 | | | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ hold time from $\overline{RD}\uparrow$ | $t_{RA}$ | 0 | | | ns | |
| $\overline{RD}$ width | $t_{RR}$ | 200 | | | ns | |
| Data access time from $\overline{RD}\downarrow$ | $t_{RD}$ | | | 140 | ns | $C_L = 100\ pF$ |
| DB to float delay time from $\overline{RD}\uparrow$ | $t_{DF}$ | 10 | | 85 | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ setup time to $\overline{WR}\downarrow$ | $t_{AW}$ | 0 | | | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ hold time to $\overline{WR}\uparrow$ | $t_{WA}$ | 0 | | | ns | |
| $\overline{WR}$ width | $t_{WW}$ | 200 | | | ns | |
| Data setup time to $\overline{WR}\uparrow$ | $t_{DW}$ | 100 | | | ns | |
| Data hold time from $\overline{WR}\uparrow$ | $t_{WD}$ | 0 | | | ns | |
| INT delay time from $\overline{RD}\uparrow$ | $t_{RI}$ | | | $2\Phi_{CY} + \Phi_0 + 135$ | ns | Non-DMA mode |
| INT delay time from $\overline{WR}\uparrow$ | $t_{WI}$ | | | $2\Phi_{CY} + \Phi_0 + 135$ | ns | |
| DRQ cycle time | $t_{MCY}$ | 13 | | | $\mu s$ | $\Phi_{CY} = 125$ ns (Note 4) |
| $\overline{DACK}\downarrow \rightarrow DRQ\downarrow$ delay | $t_{AM}$ | | | 140 | ns | |
| $DRQ\uparrow \rightarrow \overline{DACK}\downarrow$ delay | $t_{MA}$ | 200 | | | ns | $\Phi_{CY} = 125$ ns (Note 4) |
| $\overline{DACK}$ width | $t_{AA}$ | $2\Phi_{CY} + 15$ | | | ns | |
| TC width | $t_{TC}$ | 1 | | | $\Phi_{CY}$ | |
| Reset width | $t_{RST}$ | 14 | | | $\Phi_{CY}$ | |
| $DRQ\downarrow \rightarrow$ INT response time | $t_{MI}$ | 60 | | 77 | $\Phi_{CY}$ | μPD765B only |
| INT $\rightarrow \overline{DACK}$ ineffective | $t_{IA}$ | | | 1 | $\Phi_{CY}$ | |

| Parameter | Symbol | Min | Typ (1) | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| WCLK cycle time | $t_{CY}$ | | 16 | | $\Phi_{CY}$ | MFM = 0 |
| | | | 8 | | $\Phi_{CY}$ | MFM = 1 |
| WCLK active time (high) | $t_0$ | 80 | 250 | 350 | ns | Note 4 |
| CLK $\uparrow \rightarrow$ WCLK $\downarrow$ delay | $t_{CWL}$ | 0 | | $\Phi_0$ | ns | μPD765AC2 only |
| WCLK, RDATA and WINDOW rise time | $t_R$ | | | 20 | ns | |
| WCLK, RDATA and WINDOW fall time | $t_F$ | | | 20 | ns | |
| Preshift delay time from WCLK $\uparrow$ | $t_{CP}$ | 20 | | 100 | ns | |
| WCLK $\uparrow \rightarrow$ WE $\uparrow$ delay | $t_{CWE}$ | 20 | | 100 | ns | |
| WDATA delay time from WCLK $\uparrow$ | $t_{CD}$ | 20 | | 100 | ns | |
| RDATA active time (high) | $t_{RDD}$ | 40 | | | ns | |
| Window cycle time | $t_{WCY}$ | | 2 | | $\mu s$ | MFM = 0 |
| | | | 1 | | $\mu s$ | MFM = 1 |
| Window hold time from RDATA | $t_{RDW}$ | 15 | | | ns | |
| Window setup time to RDATA | $t_{WRD}$ | 15 | | | ns | |
| $US_{0,1}$ setup time to SEEK $\uparrow$ | $t_{US}$ | 12 | | | $\mu s$ | 8-MHz CLK Notes 4, 5 |
| SEEK setup time to DIR | $t_{SD}$ | 7 | | | $\mu s$ | |
| Direction setup time to step $\uparrow$ | $t_{DST}$ | 1.0 | | | $\mu s$ | |
| $US_{0,1}$ hold time from step $\uparrow$ | $t_{STU}$ | 5.0 | | | $\mu s$ | |
| Step active time (high) | $t_{STP}$ | 6 | 7 | 8 | $\mu s$ | Notes 4, 5 |
| Step cycle time | $t_{SC}$ | 33 | Note 2 | Note 2 | $\mu s$ | |
| Fault reset active time (high) | $t_{FR}$ | 8.0 | | 10 | $\mu s$ | |
| Write data width | $t_{WDD}$ | $t_0 - 50$ | | | ns | |
| $US_{0,1}$ hold time after seek | $t_{SU}$ | 15 | | | $\mu s$ | 8-MHz CLK Notes 3, 4, 5 |
| SEEK hold time from DIR | $t_{DS}$ | 30 | | | $\mu s$ | 8-MHz CLK Notes 4, 5 |
| DIR hold time after step | $t_{STD}$ | 24 | | | $\mu s$ | |
| Index pulse width | $t_{IDX}$ | 4 | | | $\Phi_{CY}$ | |

## AC Characteristics (cont)

| Parameter | Symbol | Min | Typ (1) | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| $\overline{RD}$ ↓ delay from DRQ | $t_{MR}$ | 800 | | | ns | 8-MHz CLK Note 4 |
| $\overline{WR}$ ↓ delay from DRQ | $t_{MW}$ | 250 | | | ns | |
| $\overline{WR}$ ↑ or $\overline{RD}$ ↑ response time from DRQ ↑ | $t_{MRW}$ | | | 12 | µs | |

**Notes:**

(1) Typical values for $T_A = 25°C$ and nominal supply voltage.

(2) Under software control. The range is from 1 ms to 16 ms at 8-MHz clock period, and 2 ms to 32 ms at 4-MHz clock period.

(3) When one device is executing a SEEK operation, SENSE DRIVE STATUS is executed on another device.

(4) Double these values for a 4-MHz clock period.

(5) The drive side rating has a variance of −50 ns from the minimum value.

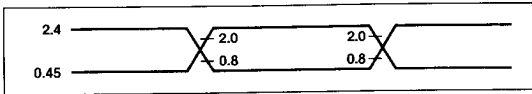## Timing Waveforms
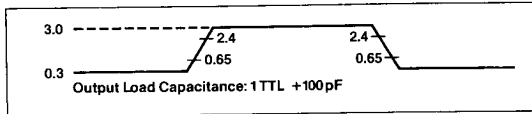
### Processor Read Operation
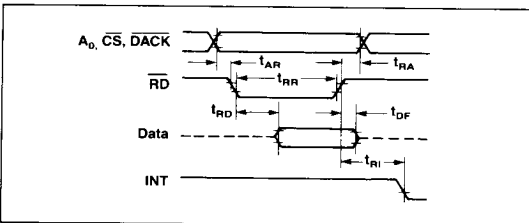


### Processor Write Operation
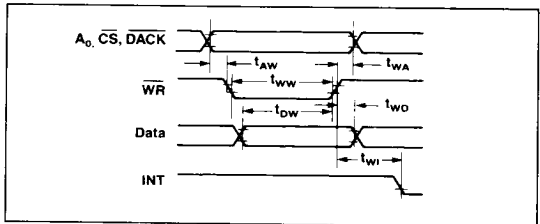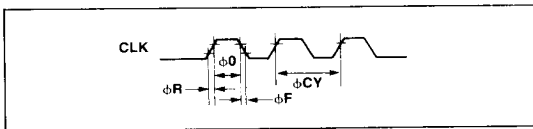
## Timing Waveforms (Cont)

### Data Input Waveform for AC Test (Except CLK, WCLK)



### Clock (WCLK, CLK) Input Waveform for AC Test



Output Load Capacitance: 1 TTL +100 pF

### Clock



### DMA Operation



### FDD Write Operation



|           | Preshift 0 | Preshift 1 |
|-----------|-----------|-----------|
| Normal    | 0         | 0         |
| Late      | 0         | 1         |
| Early     | 1         | 0         |
| Invalid   | 1         | 1         |
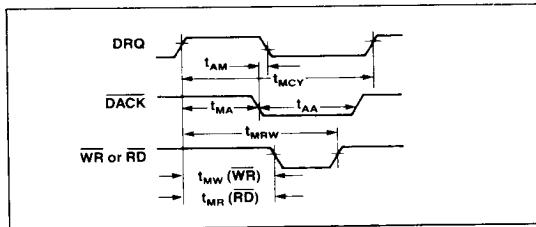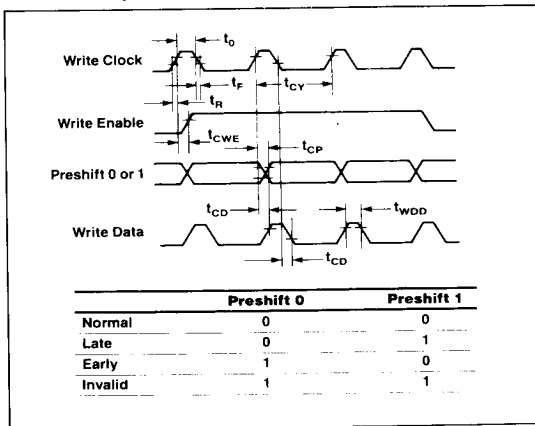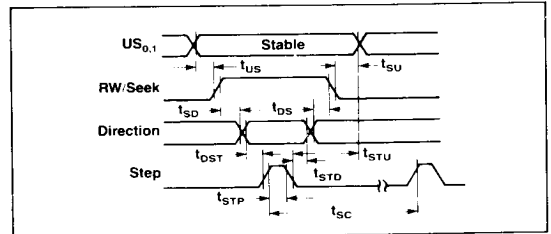
### Seek Operation



### Overrun Operation (μPD765B Only)
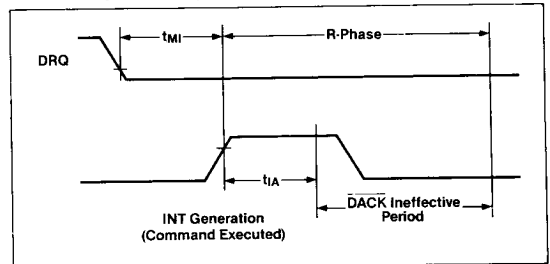


### FLT Reset
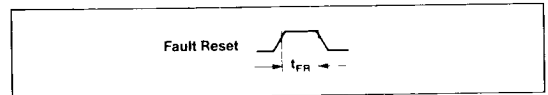


### FDD Read Operation



**Note:** Either polarity data window is valid.
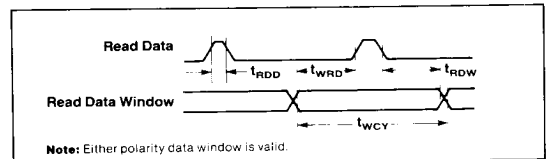
### Terminal Count
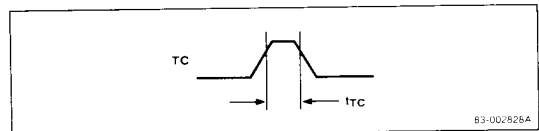


### Reset

## Timing Waveforms (Cont)

### Write Clock



### Index



## Internal Registers

The μPD765A/μPD765B contains two registers which may be accessed by the main system processor: a status register and a data register. The 8-bit main status register contains the status information of the FDC, and may be accessed at any time. The 8-bit data register (which actually consists of four registers, ST0–ST3, in a stack with only one register presented to the data bus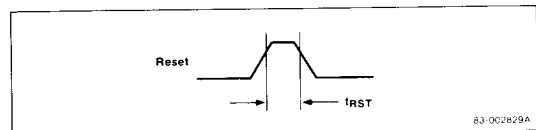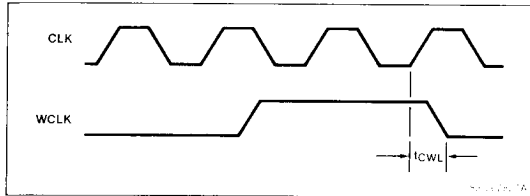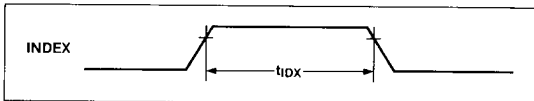 at a time), stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the data register in order to program or obtain the results after a particular command (table 3). Only the status register may be read and used to facilitate the transfer of data between the processor and μPD765A/μPD765B.

The relationship between the status/data registers and the signals $\overline{RD}$, $\overline{WR}$, and $A_0$ is shown in table 1.

### Table 1. Status/Data Register Addressing

| $A_0$ | $\overline{RD}$ | $\overline{WR}$ | Function |
|---|---|---|---|
| 0 | 0 | 1 | Read main status register |
| 0 | 1 | 0 | Illegal |
| 0 | 0 | 0 | Illegal |
| 1 | 0 | 0 | Illegal |
| 1 | 0 | 1 | Read from data register |
| 1 | 1 | 0 | Write into data register |

The bits in the main status register are defined in table 2.

### Table 2. Main Status Register

| Pin No. | Name | Function |
|---|---|---|
| $DB_0$ | $D_0B$ (FDD 0 Busy) | FDD number 0 is in the seek mode. If any of the $D_nB$ bits is set FDC will not accept read or write command. |
| $DB_1$ | $D_1B$ (FDD 1 Busy) | FDD number 1 is in the seek mode. If any of the $D_nB$ bits is set FDC will not accept read or write command. |
| $DB_2$ | $D_2B$ (FDD 2 Busy) | FDD number 2 is in the seek mode. If any of the $D_nB$ bits is set FDC will not accept read or write command. |
| $DB_3$ | $D_3B$ (FDD 3 Busy) | FDD number 3 is in the seek mode. If any of the $D_nB$ bits is set FDC will not accept read or write command. |
| $DB_4$ | CB (FDC Busy) | A Read or Write command is in process. FDC will not accept any other command. |
| $DB_5$ | EXM (Execution Mode) | This bit is set only during execution phase in non-DMA mode. When $DB_5$ goes low, execution phase has ended and result phase has started. It operates only during non-DMA mode of operation. |
| $DB_6$ | DIO (Data Input / Output) | Indicates direction of data transfer between FDC and data register. If DIO = 1, then transfer is from data register to the processor. If DIO = 0, then transfer is from the processor to data register. |
| $DB_7$ | RQM (Request for Master) | Indicates data register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor. |

The DIO and RQM bits in the status register indicate when data is ready and in which direction data will be transferred on the data bus. See figure 1.

### Figure 1. DIO and RQM

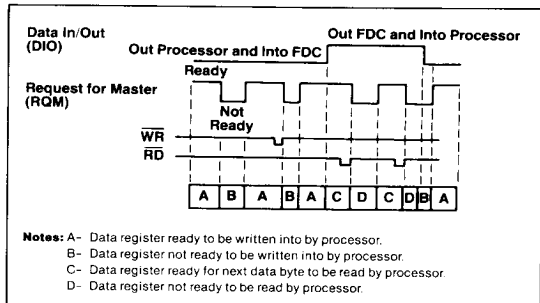

**Notes:** A– Data register ready to be written into by processor.
B– Data register not ready to be written into by processor.
C– Data register ready for next data byte to be read by processor.
D– Data register not ready to be read by processor.

## Table 3.  Status Register Identification

| Pin | | Function |
|---|---|---|
| No. | Name | |
| **Status Register 0** | | |
| $D_7$, $D_6$ | IC (Interrupt Code) | $D_7 = 0$ and $D_6 = 0$<br>Normal termination of command, (NT). Command was completed and properly executed. |
| | | $D_7 = 0$ and $D_6 = 1$<br>Abnormal termination of command, (AT). Execution of command was started but was not successfully completed. |
| | | $D_7 = 1$ and $D_6 = 0$<br>Invalid command issue, (IC). Command which was issued was never started. |
| | | $D_7 = 1$ and $D_6 = 1$<br>Abnormal termination because during command execution the ready signal from FDD changed state. |
| $D_5$ | SE (Seek End) | When the FDC completes the Seek command, this flag is set to 1 (high). |
| $D_4$ | EC (Equipment Check) | If a fault signal is received from the FDD, or if the track 0 signal fails to occur after 77 step pulses (Recalibrate Command) then this flag is set. |
| $D_3$ | NR (Not Ready) | When the FDD is in the not-ready state and a Read or Write command is issued, this flag is set. If a Read or Write command is issued to side 1 of a single-sided drive, then this flag is set. |
| $D_2$ | HD (Head Address) | This flag is used to indicate the state of the head at interrupt. |
| $D_1$ | $US_1$ (Unit Select 1) | This flag is used to indicate a drive unit number at interrupt. |
| $D_0$ | $US_0$ (Unit Select 0) | This flag is used to indicate a drive unit number at interrupt. |
| **Status Register 1** | | |
| $D_7$ | EN (End of Cylinder) | When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set. |
| $D_6$ | | Not used. This bit is always 0 (low). |
| $D_5$ | DE (Data Error) | When the FDC detects a CRC(1) error in either the ID field or the data field, this flag is set. |
| $D_4$ | OR (Overrun) | If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set. |
| $D_3$ | | Not used. This bit is always 0 (low). |

## Table 3.  Status Register Identification (cont)

| Pin | | Function |
|---|---|---|
| No. | Name | |
| **Status Register 1 (cont)** | | |
| $D_2$ | ND (No Data) | During execution of Read Data, Read Deleted Data, Write Data, Write Deleted Data or Scan command, if the FDC cannot find the sector specified in the IDR(2) Register, this flag is set. |
| | | During execution of the Read ID command, if the FDC cannot read the ID field without an error, then this flag is set. |
| | | During execution of the Read Diagnostic command, if the starting sector cannot be found, then this flag is set. |
| $D_1$ | NW (Not Writable) | During execution of Write Data, Write Deleted Data or Write ID command, if the FDC detects a write protect signal from the FDD, then this flag is set. |
| $D_0$ | MA (Missing Address Mark) | This bit is set if the FDC does not detect the IDAM before 2 index pulses. It is also set if the FDC cannot find the DAM or DDAM after the IDAM is found, MD bit of ST2 is also set at this time. |
| **Status Register 2** | | |
| $D_7$ | | Not used. This bit is always 0 (low). |
| $D_6$ | CM (Control Mark) | During execution of the Read Data or Scan command, if the FDC encounters a sector which contains a deleted data address mark, this flag is set. Also set if DAM is found during Read Deleted Data. |
| $D_5$ | DD (Data Error in Data Field) | If the FDC detects a CRC error in the data field then this flag is set. |
| $D_4$ | WC (Wrong Cylinder) | This bit is related to the ND bit, and when the contents of C(3) on the medium is different from that stored in the IDR, this flag is set. |
| $D_3$ | SH (Scan Equal Hit) | During execution of the Scan command, if the condition of "equal" is satisfied, this flag is set. |
| $D_2$ | SN (Scan Not Satisfied) | During execution of the Scan command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set. |
| $D_1$ | BC (Bad Cylinder) | This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FFH, then this flag is set. |
| $D_0$ | MD (Missing Address Mark in Data Field) | When data is read from the medium, if the FDC cannot find a data address mark or deleted data address mark, then this flag is set. |

## Table 3. Status Register Identification (cont)

| No. | Name | Function |
|-----|------|----------|
| **Pin** | | |
| **Status Register 3** | | |
| $D_7$ | FT (Fault) | This bit is used to indicate the status of the fault signal from the FDD. |
| $D_6$ | WP (Write Protected) | This bit is used to indicate the status of the write protected signal from the FDD. |
| $D_5$ | RY (Ready) | This bit is used to indicate the status of the ready signal from the FDD. |
| $D_4$ | T0 (Track 0) | This bit is used to indicate the status of the track 0 signal from the FDD. |
| $D_3$ | TS (Two-Side) | This bit is used to indicate the status of the two-side signal from the FDD. |
| $D_2$ | HD (Head Address) | This bit is used to indicate the status of the side select signal to the FDD. |
| $D_1$ | US$_1$ (Unit Select 1) | This bit is used to indicate the status of the unit select 1 signal to the FDD. |
| $D_0$ | US$_0$ (Unit Select 0) | This bit is used to indicate the status of the unit select 0 signal to the FDD. |

**Note:**

(1) CRC = Cyclic Redundancy Check
(2) IDR = Internal Data Register
(3) Cylinder (C) is described more fully in the Command Symbol Description.

## Command Sequence

The μPD765A/μPD765B is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the μPD765A/μPD765B and the processor, it is convenient to consider each command as consisting of three phases:

| | |
|---|---|
| Command Phase: | The FDC receives all information required to perform a particular operation from the processor. |
| Execution Phase: | The FDC performs the operation it was instructed to do. |
| Result Phase: | After completion of the operation, status and other housekeeping information are made available to the processor. |

Table 4 shows the required preset parameters and results for each command. Most commands require 9 command bytes and return 7 bytes during the result phase. The "W" to the left of each byte indicates a command phase byte to be written, and an "R" indicates a result byte. The definitions of other abbriviations used in table are given in the Command Symbol Description table.

## Command Symbol Description

| Name | Function |
|------|----------|
| $A_0$ (Address Line 0) | $A_0$ controls selection of main status register ($A_0 = 0$) or data register ($A_0 = 1$). |
| C (Cylinder Number) | C stands for the current / selected cylinder (track) numbers 0 through 76 of the medium. |
| D (Data) | D stands for the data pattern which is going to be written into a sector during WRITE ID operation. |
| $D_7$–$D_0$ (Data Bus) | 8-bit data bus, where $D_7$ stands for a most significant bit, and $D_0$ stands for a least significant bit. |
| DTL (Data Length) | When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector. |
| EOT (End of Track) | EOT stands for the final sector number on a cylinder. During read or write operations, FDC will stop data transfer after a sector number equal to EOT. |
| GPL (Gap Length) | GPL stands for the length of gap 3. During Read / Write commands this value determines the number of bytes that VCO sync will stay low after two CRC bytes. During Format command it determines the size of gap 3. |
| H (Head Address) | H stands for the logical head number 0 or 1, as specified in ID field. |
| HD (Head) | HD stands for a the physical head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.) |
| HLT (Head Load Time) | HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments). |
| HUT (Head Unload Time) | HUT stands for the head unload time after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments). |
| MF (FM or MFM Mode) | If MF is low, FM mode is selected, and if it is high, MFM mode is selected. |
| MT (Multitrack) | IF MT is high, a multitrack operation is performed. If MT = 1 after finishing read / write operation on side 0, FDC will automatically start searching for sector 1 on side 1. |
| N (Number) | N stands for the number of data bytes written in a sector. |
| NCN (New Cylinder Number) | NCN stands for a new cylinder number which is going to be reached as a result of the seek operation; desired position of head. |
| ND (Non-DMA Mode) | ND stands for operation in the non-DMA mode. |
| PCN (Present Cylinder Number) | PCN stands for the cylinder number at the completion of Sense Interrupt Status command, position of head at present time. |
| R (Record) | R stands for the sector number which will be read or written. |
| R/W (Read / Write) | R/W stands for either Read (R) or Write (W) signal. |
| SC (Sector) | SC indicates the number of sectors per cylinder. |
| SK (Skip) | SK stands for skip deleted data address mark. |

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## Command Symbol Description (cont)

| Name | Function |
|---|---|
| SRT (Step Rate Time) | SRT stands for the stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (FH = 1 ms, EH = 2 ms, etc.). |
| ST0–ST3 (Status 0–3) | ST0–ST3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0 = 0$). ST0–ST3 may be read only after a command has been executed and contains information relevant to that particular command. |

## Command Symbol Description (cont)

| Name | Function |
|---|---|
| STP | During a scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared. |
| $US_0$, $US_1$ (Unit Select) | US stands for a selected drive number 0 or − 3. |

## Table 4.  Instruction Set (Notes 1, 2)

| Phase | R/W | D₇ | D₆ | D₅ | D₄ | D₃ | D₂ | D₁ | D₀ | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| **Read Data** | | | | | | | | | | |
| Command | W | MT | MF | SK | 0 | 0 | 1 | 1 | 0 | Command codes |
| | W | X | X | X | X | X | HD | US₁ | US₀ | (Note 3) |
| | W | | | | C | | | | | Sector ID information prior to command execution. The 4 bytes |
| | W | | | | H | | | | | are compared against header on floppy disk. |
| | W | | | | R | | | | | |
| | W | | | | N | | | | | |
| | W | | | | EOT | | | | | |
| | W | | | | GPL | | | | | |
| | W | | | | DTL | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and main system |
| Result | R | | | | ST 0 | | | | | Status information after command execution |
| | R | | | | ST 1 | | | | | |
| | R | | | | ST 2 | | | | | |
| | R | | | | C | | | | | Sector ID information after command execution |
| | R | | | | H | | | | | |
| | R | | | | R | | | | | |
| | R | | | | N | | | | | |
| **Read Deleted Data** | | | | | | | | | | |
| Command | W | MT | MF | SK | 0 | 1 | 1 | 0 | 0 | Command codes |
| | W | X | X | X | X | X | HD | US₁ | US₀ | |
| | W | | | | C | | | | | Sector ID information prior to command execution. The 4 bytes |
| | W | | | | H | | | | | are compared against header on floppy disk. |
| | W | | | | R | | | | | |
| | W | | | | N | | | | | |
| | W | | | | EOT | | | | | |
| | W | | | | GPL | | | | | |
| | W | | | | DTL | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and main system |
| Result | R | | | | ST 0 | | | | | Status information after command execution |
| | R | | | | ST 1 | | | | | |
| | R | | | | ST 2 | | | | | |
| | R | | | | C | | | | | Sector ID information after command execution |
| | R | | | | H | | | | | |
| | R | | | | R | | | | | |
| | R | | | | N | | | | | |

**Note:**

(1) Symbols used in this table are described at the end of this section.

(2) $A_0$ should equal 1 for all operations.

(3) X = Don't care, usually made to equal 0.

## Table 4. Instruction Set (Notes 1, 2) (cont)

| Phase | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Remarks |
|-------|-----|----|----|----|----|----|----|----|----|---------|
| **Write Data** | | | | | | | | | | |
| Command | W | MT | MF | 0 | 0 | 0 | 1 | 0 | 1 | Command codes |
| | W | X | X | X | X | X | HD | US$_1$ | US$_0$ | |
| | W | ← | | | C | | | | → | Sector ID information prior to command execution. The 4 bytes |
| | W | ← | | | H | | | | → | are compared against header on floppy disk. |
| | W | ← | | | R | | | | → | |
| | W | ← | | | N | | | | → | |
| | W | ← | | | EOT | | | | → | |
| | W | ← | | | GPL | | | | → | |
| | W | ← | | | DTL | | | | → | |
| Execution | | | | | | | | | | Data transfer between the main system and FDD |
| Result | R | ← | | | ST 0 | | | | → | Status information after command execution |
| | R | ← | | | ST 1 | | | | → | |
| | R | ← | | | ST 2 | | | | → | |
| | R | ← | | | C | | | | → | Sector ID information after command execution |
| | R | ← | | | H | | | | → | |
| | R | ← | | | R | | | | → | |
| | R | ← | | | N | | | | → | |
| **Write Deleted Data** | | | | | | | | | | |
| Command | W | MT | MF | 0 | 0 | 1 | 0 | 0 | 1 | Command codes |
| | W | X | X | X | X | X | HD | US$_1$ | US$_0$ | |
| | W | ← | | | C | | | | → | Sector ID information prior to command execution. The 4 bytes |
| | W | ← | | | H | | | | → | are compared against header on floppy disk. |
| | W | ← | | | R | | | | → | |
| | W | ← | | | N | | | | → | |
| | W | ← | | | EOT | | | | → | |
| | W | ← | | | GPL | | | | → | |
| | W | ← | | | DTL | | | | → | |
| Execution | | | | | | | | | | Data transfer between the FDD and main system |
| Result | R | ← | | | ST 0 | | | | → | Status information after command execution |
| | R | ← | | | ST 1 | | | | → | |
| | R | ← | | | ST 2 | | | | → | |
| | R | ← | | | C | | | | → | Sector ID information after command execution |
| | R | ← | | | H | | | | → | |
| | R | ← | | | R | | | | → | |
| | R | ← | | | N | | | | → | |
| **Read Diagnostic** | | | | | | | | | | |
| Command | W | 0 | MF | SK | 0 | 0 | 0 | 1 | 0 | Command codes |
| | W | X | X | X | X | X | HD | US$_1$ | US$_0$ | |
| | W | ← | | | C | | | | → | Sector ID information prior to command execution |
| | W | ← | | | H | | | | → | |
| | W | ← | | | R | | | | → | |
| | W | ← | | | N | | | | → | |
| | W | ← | | | EOT | | | | → | |
| | W | ← | | | GPL | | | | → | |
| | W | ← | | | DTL | | | | → | |
| Execution | | | | | | | | | | Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT. |
| Result | R | ← | | | ST 0 | | | | → | Status information after command execution |
| | R | ← | | | ST 1 | | | | → | |
| | R | ← | | | ST 2 | | | | → | |
| | R | ← | | | C | | | | → | Sector ID information after command execution |
| | R | ← | | | H | | | | → | |
| | R | ← | | | R | | | | → | |
| | R | ← | | | N | | | | → | |

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## Table 4. Instruction Set (Notes 1, 2) (cont)

| Phase | R/W | D₇ | D₆ | D₅ | D₄ | D₃ | D₂ | D₁ | D₀ | Remarks |
|-------|-----|----|----|----|----|----|----|----|----|---------|
| **Read ID** | | | | | | | | | | |
| Command | W | 0 | MF | 0 | 0 | 1 | 0 | 1 | 0 | Command codes |
| | W | X | X | X | X | X | HD | US₁ | US₀ | |
| Execution | | | | | | | | | | The first correct ID information on the cylinder is stored in data register. |
| Result | R | ← ST 0 → | | | | | | | | Status information after command execution |
| | R | ← ST 1 → | | | | | | | | |
| | R | ← ST 2 → | | | | | | | | |
| | R | ← C → | | | | | | | | Sector ID information read during execution phase from floppy disk. |
| | R | ← H → | | | | | | | | |
| | R | ← R → | | | | | | | | |
| | R | ← N → | | | | | | | | |
| **Write ID [Format Write]** | | | | | | | | | | |
| Command | W | 0 | MF | 0 | 0 | 1 | 1 | 0 | 1 | Command codes |
| | W | X | X | X | X | X | HD | US₁ | US₀ | |
| | W | ← N → | | | | | | | | Bytes / sector |
| | W | ← SC → | | | | | | | | Sectors / track |
| | W | ← GPL → | | | | | | | | Gap 3 |
| | W | ← D → | | | | | | | | Filler byte |
| Execution | | | | | | | | | | FDC formats an entire track. |
| Result | R | ← ST 0 → | | | | | | | | Status information after command execution |
| | R | ← ST 1 → | | | | | | | | |
| | R | ← ST 2 → | | | | | | | | |
| | R | ← C → | | | | | | | | In this case, the ID information has no meaning |
| | R | ← H → | | | | | | | | |
| | R | ← R → | | | | | | | | |
| | R | ← N → | | | | | | | | |
| **Scan Equal** | | | | | | | | | | |
| Command | W | MT | MF | SK | 1 | 0 | 0 | 0 | 1 | Command codes |
| | W | X | X | X | X | X | HD | US₁ | US₀ | |
| | W | ← C → | | | | | | | | Sector ID information prior to command execution |
| | W | ← H → | | | | | | | | |
| | W | ← R → | | | | | | | | |
| | W | ← N → | | | | | | | | |
| | W | ← EOT → | | | | | | | | |
| | W | ← GPL → | | | | | | | | |
| | W | ← STP → | | | | | | | | |
| Execution | | | | | | | | | | Data compared between the FDD and main system |
| Result | R | ← ST 0 → | | | | | | | | Status information after command execution |
| | R | ← ST 1 → | | | | | | | | |
| | R | ← ST 2 → | | | | | | | | |
| | R | ← C → | | | | | | | | Sector ID information after command execution |
| | R | ← H → | | | | | | | | |
| | R | ← R → | | | | | | | | |
| | R | ← N → | | | | | | | | |

**Note:**
(1) Symbols used in this table are described at the end of this section.
(2) $A_0$ should equal 1 for all operations.
(3) X = Don't care, usually made to equal 0.

### Table 4. Instruction Set (Notes 1, 2)(cont)

| Phase | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Remarks |
|-------|-----|----|----|----|----|----|----|----|----|---------|
| **Scan Low or Equal** | | | | | | | | | | |
| Command | W | MT | MF | SK | 1 | 1 | 0 | 0 | 1 | Command codes |
| | W | X | X | X | X | X | HD | $US_1$ | $US_0$ | |
| | W | ← | | | | C | | | → | Sector ID information prior to command execution |
| | W | ← | | | | H | | | → | |
| | W | ← | | | | R | | | → | |
| | W | ← | | | | N | | | → | |
| | W | ← | | | | EOT | | | → | |
| | W | ← | | | | GPL | | | → | |
| | W | ← | | | | STP | | | → | |
| Execution | | | | | | | | | | Data compared between the FDD and main system |
| Result | R | ← | | | | ST 0 | | | → | Status information after command execution |
| | R | ← | | | | ST 1 | | | → | |
| | R | ← | | | | ST 2 | | | → | |
| | R | ← | | | | C | | | → | Sector ID information after command execution |
| | R | ← | | | | H | | | → | |
| | R | ← | | | | R | | | → | |
| | R | ← | | | | N | | | → | |
| **Scan High or Equal** | | | | | | | | | | |
| Command | W | MT | MF | SK | 1 | 1 | 1 | 0 | 1 | Command codes |
| | W | X | X | X | X | X | HD | $US_1$ | $US_0$ | |
| | W | ← | | | | C | | | → | Sector ID information prior to command execution |
| | W | ← | | | | H | | | → | |
| | W | ← | | | | R | | | → | |
| | W | ← | | | | N | | | → | |
| | W | ← | | | | EOT | | | → | |
| | W | ← | | | | GPL | | | → | |
| | W | ← | | | | STP | | | → | |
| Execution | | | | | | | | | | Data compared between the FDD and main system |
| Result | R | ← | | | | ST 0 | | | → | Status information after command execution |
| | R | ← | | | | ST 1 | | | → | |
| | R | ← | | | | ST 2 | | | → | |
| | R | ← | | | | C | | | → | Sector ID information after command execution |
| | R | ← | | | | H | | | → | |
| | R | ← | | | | R | | | → | |
| | R | ← | | | | N | | | → | |
| **Recalibrate** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | Command codes |
| | W | X | X | X | X | X | 0 | $US_1$ | $US_0$ | |
| Execution | | | | | | | | | | Head retracted to track 0 |
| **Sense Interrupt Status** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Command codes |
| Result | R | ← | | | | ST 0 | | | → | Status information about the FDC at the end of seek operation |
| | R | ← | | | | PCN | | | → | |
| **Specify** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Command codes |
| | W | ← | SRT | | → | ← | HUT | | → | |
| | W | ← | | HLT | | | | → | ND | |
| **Sense Drive Status** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Command codes |
| | W | X | X | X | X | X | HD | $US_1$ | $US_0$ | |
| Result | R | ← | | | | ST 3 | | | → | Status information about FDD |

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*Table 4. Instruction Set (Notes 1, 2) (cont)*

| Phase | R/W | D₇ | D₆ | D₅ | D₄ | D₃ | D₂ | D₁ | D₀ | Remarks |
|-------|-----|----|----|----|----|----|----|----|----|---------|
| **Version** | | | | | | | | | | |
| Command | W | X | X | X | 1 | 0 | 0 | 0 | 0 | Command codes |
| Result | R | ← | | | ST 0 | | | | → | 90H indicates 765B<br>80H indicates 765A / A–2 |
| **Seek** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | Command code |
|  | W | X | X | X | X | X | HD | US₁ | US₀ | |
|  | W | ← | | | NCN | | | | → | |
| Execution | | | | | | | | | | Head is positioned over proper cylinder on diskette |
| **Invalid** | | | | | | | | | | |
| Command | W | ← | | | Invalid Codes | | | | → | Invalid Command codes (No op — FDC goes into state) |
| Result | R | ← | | | ST 0 | | | | → | ST 0 = 80H |

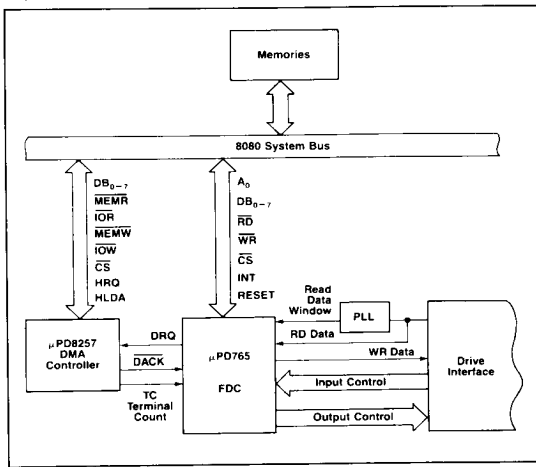**Note:**

(1) Symbols used in this table are described at the end of this section.

(2) $A_0$ should equal 1 for all operations.

(3) X = Don't care, usually made to equal 0.

## System Configuration

Figure 2 shows an example of a system using a μPD765A/B.

*Figure 2. System Configuration*

## Data Format

Figure 3 shows the data transfer format for the µPD765A and µPD765B in FM and MFM modes. Figure 4 shows VCO Sync timing.

*Figure 3. Data Format*



*µPD765A/B [FM Mode]*

| GAP 4a 40x FF | SYNC 6x 00 | IAM FC | GAP 1 26x FF | SYNC 6x 00 | IDAM FE | C Y L | H D | S E C | N O | C R C | GAP 2 11x FF | SYNC 6x 00 | DATA AM FB or F8 | DATA (1) | C R C | GAP 3 (1) | GAP 4b |

Index — Repeat N Times

*µPD765A/B [MFM Mode]*

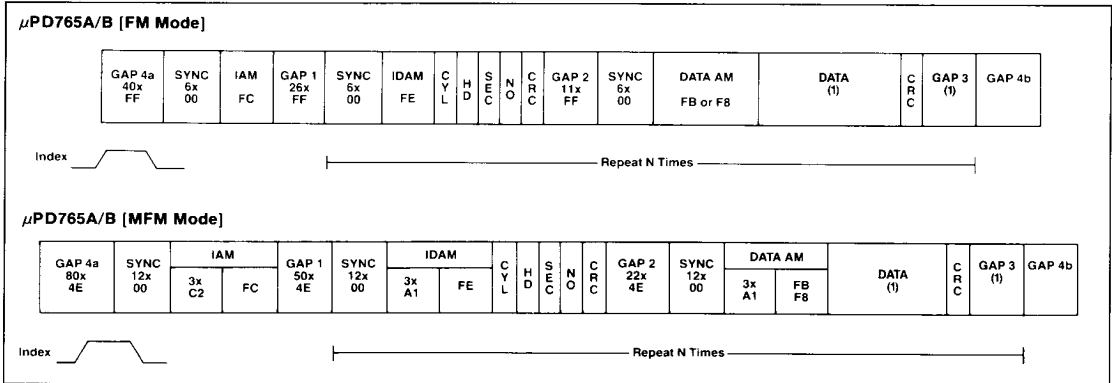| GAP 4a 80x 4E | SYNC 12x 00 | IAM 3x C2 | FC | GAP 1 50x 4E | SYNC 12x 00 | IDAM 3x A1 | FE | C Y L | H D | S E C | N O | C R C | GAP 2 22x 4E | SYNC 12x 00 | DATA AM 3x A1 | FB F8 | DATA (1) | C R C | GAP 3 (1) | GAP 4b |

Index — Repeat N Times

*Figure 4. VCO Sync Timing*



µPD765A/B