TND309

General Information for MECL 10H™ and MECL 10K™

ON Semiconductor®

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APPLICATION NOTE

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HIGH–SPEED LOGIC

High speed logic is used whenever improved system performance would increase a product's market value. For a given system design, high–speed logic is the most direct way to improve system performance and Emitter–Coupled Logic (ECL) is one of today's fastest forms of digital logic. Emitter– coupled logic offers both the logic speed and logic features to meet the market demands for higher performance systems.

MECL Products

ON Semiconductor (formerly a division of Motorola SPS), introduced the original monolithic emitter–coupled logic family with MECL I (1962) and followed this with MECL II (1966). These two families are now obsolete and have given way to the MECL III™ (MC1600 series), MECL 10K™, PLL (MC12000 series) and the new MECL 10H™ families.

Chronologically the third family introduced, MECL III (1968) is a higher power, higher speed logic. Typical 1.0 ns edge speeds and propagation delays along with greater than 500 MHz flip–flop toggle rates, make MECL III useful for high–speed test and communications equipment. Also, this family is used in the high–speed sections and critical timing delays of larger systems. For more general purpose applications, however, trends in large high–speed systems showed the need for an easy–to–use logic family with propagation delays on the order of 2.0 ns. To match this requirement, the MECL™ 10,000 Series was introduced in 1971.

An important feature of MECL 10K is its compatibility with MECL III to facilitate using both families in the same system. A second important feature is its significant power economy – MECL 10K gates use less than one–half the power of MECL III.

The MECL 10H product family was introduced in 1981. This latest MECL family features 100% improvements in propagation delay and clock speeds while maintaining power supply currents equal to MECL 10K. MECL 10H is voltage compensated allowing guaranteed DC and switching parameters over a ±5% power supply range. Noise margins have been improved by 75% over the MECL 10K series.

Compatibility with MECL 10K and MECL III is a key element in allowing users to enhance existing systems by increasing the speed in critical timing areas. Also, many MECL 10H devices are pin out/functional duplications of the MECL 10K series devices. The emphasis of this family will be placed on more powerful logic functions having more complexity and greater performance. With 1.0 ns propagation delays and 25 mW per gate, MECL 10H is one of the best speed–power families of any ECL logic family available today.

MECL at +5.0 V (PECL – Positive ECL)

Any single supply ECL device is also a PECL device, making the PECL portfolio as large as the existing ECL one. (Note: The dual supply translator devices cannot operate at +5.0 V and ground and cannot be considered PECL devices.)

ECL devices in the PECL mode, must have the input/output DC specifications adjusted for proper operation. ECL levels (DC) are referenced from the V_{CC} level. To calculate the PECL DC specifications, ECL levels are added to the new V_{CC}.

Example:

PECL V_{OH} = New V_{CC} + ECL V_{OH}, 5.0 V + (–0.81 V) = 4.190 V and is the max V_{OH} level at 25°C for a PECL device. Follow the same procedure to calculate all input/output DC specifications for a device used in a PECL mode. The V_{TT} supply used to sink the parallel termination currents is also referenced from the V_{CC} supply and is V_{CC} – 2.0 V. The PECL V_{TT} supply = +5.0 V – 2.0 V = +3.0 V and should track the V_{CC} supply one–to–one for specified operation.

Since ECL is referenced from the V_{CC} rail, any noise on the V_{CC} supply will be reflected on the output waveshape at a one–to–one ratio. Therefore, noise should be kept as low as possible for best operation. Devices in a PECL system cannot have V_{CC} vary more than 5% to assure proper AC operation. See ON Semiconductor Application Note AN1406/D "*Designing With PECL (ECL at +5.0 V)*" for more details.

AC performance in the PECL mode is equal to the AC performance in the ECL mode, if the pitfalls set forth in Application Note (AN1406/D) are avoided.

MECL FAMILY COMPARISONS

Table 1. General Characteristics

Feature	MECL 10H	MECL 10K	
		10,100 Series	10,200 Series
1. Gate Propagation Delay	1.0 ns	2.0 ns	1.5 ns
2. Output Edge Speed*	1.0 ns	3.5 ns	2.5 ns
3. Flip–Flop Toggle Speed	250 MHz min	125 MHz min	200 MHz min
4. Gate Power	25 mW	25 mW	25 mW
5. Speed Power Product	25 pJ	50 pJ	37 pJ

*Output edge speed: MECL 10K/10H measured 20% to 80%.

Table 2. Operating Temperature Range

Ambient Temperature Range	MECL 10H	MECL 10K
0° to 75°C	MC10H100 Series	
–30°C to +85°C		MC10100 Series MC10200 Series

MECL IN PERSPECTIVE

In evaluating any logic line, speed and power requirements are the obvious primary considerations. Table 1 and Table 2 provide the basic parameters of the MECL 10H, MECL 10K, and MECL III families. But these provide only the start of any comparative analysis, as there are a number of other important features that make MECL highly desirable for system implementation. Among these:

Complementary Outputs cause a function and its complement to appear simultaneously at the device outputs, without the use of external inverters. It reduces package count by eliminating the need for associated invert functions and, at the same time, cuts system power requirements and reduces timing differential problems arising from the time delays introduced by inverters.

High Input Impedance and Low Output Impedance permit large fan out and versatile drive characteristics.

Insignificant Power Supply Noise Generation, due to differential amplifier design which eliminates current spikes even during signal transition period.

Nearly Constant Power Supply Current Drain simplifies power–supply design and reduces costs.

Low Cross–Talk due to low–current switching in signal path and small (typically 850 mV) voltage swing, and to relatively long rise and fall times.

Wide Variety of Functions, including complex functions facilitated by low power dissipation (particularly in MECL 10H and MECL 10K series). A basic MECL 10K gate consumes less than 8.0 mW in on–chip power in some complex functions.

Wide Performance Flexibility due to differential amplifier design which permits MECL circuits to be used as linear as well as digital circuits.

Transmission Line Drive Capability is afforded by the open emitter outputs of MECL devices. No “Line Drivers” are listed in MECL families, because *every* device is a line driver.

Wire–ORing reduces the number of logic devices required in a design by producing additional OR gate functions with only an interconnection.

Twisted Pair Drive Capability permits MECL circuits to drive twisted–pair transmission lines as long as 1000 feet.

Wire–Wrap Capability is possible with the MECL 10K family because of the slow rise and fall time characteristic of the circuits.

Open Emitter–Follower Outputs are used for MECL outputs to simplify signal line drive. The outputs match any line impedance and the absence of internal pulldown resistors saves power.

Input Pulldown Resistors of approximately 50 kΩ permit unused inputs to remain unconnected for easier circuit board layout.

MECL APPLICATIONS

ON Semiconductor’s MECL product lines are designed for a wide range of systems needs. Within the computer market, MECL 10K is used in systems ranging from special purpose peripheral controllers to large mainframe computers. Big growth areas in this market include disk and communication channel controllers for larger systems and high performance minicomputers.

The industrial market primarily uses MECL for high performance test systems such as IC or PC board testers. However, the high bandwidths of MECL 10H and MECL 10K are required for many frequency synthesizer systems using high speed phase lock loop networks. MECL has continued to grow in the industrial market through complex medical electronic products and high performance process control systems.

BASIC CONSIDERATIONS FOR HIGH–SPEED LOGIC DESIGN

High–speed operation involves only four considerations that differ significantly from operation at low and medium speeds:

1. Time delays through interconnect wiring, which may have been ignored in medium–speed systems, become highly important at state–of–the–art speeds.
2. The possibility of distorted waveforms due to reflections on signal lines increases with edge speed.
3. The possibility of “crosstalk” between adjacent signal leads is proportionately increased in high–speed systems.
4. Electrical noise generation and pick–up are more detrimental at higher speeds.

In general, these four characteristics are speed– and frequency–dependent, and are virtually independent of the type of logic employed. The merit of a particular logic family is measured by how well it compensates for these deleterious effects in system applications.

The interconnect–wiring time delays can be reduced only by reducing the length of the interconnecting lines. At logic speeds of two nanoseconds, an equivalent “gate delay” is introduced by every foot of interconnecting wiring. Obviously, for functions interconnected within a single monolithic chip, the time delays of signals travelling from one function to another are insignificant. But for a great many externally interconnected parts, this can soon add up to an appreciable delay time. Hence, the greater the number of functions per chip, the higher the system speed. *MECL circuits, particularly those of the MECL 10K and MECL 10H Series are designed with a propensity toward complex functions to enhance overall system speed.*

Waveform distortion due to line reflections also becomes troublesome principally at state–of–the–art speeds. At slow and medium speeds, reflections on interconnecting lines are not usually a serious problem. At higher speeds, however, line lengths can approach the wavelength of the signal and improperly terminated lines can result in reflections that will cause false triggering (see Figures 1 and 2). The solution, as in RF technology, is to employ “transmission–line” practices and properly terminate each signal line with its characteristic impedance at the end of its run. *The low–impedance, emitter–follower outputs of MECL circuits facilitate transmission–line practices without upsetting the voltage levels of the system.*

The increased affinity for crosstalk in high–speed circuits is the result of very steep leading and trailing edges (fast rise and fall times) of the high–speed signal. These steep wavefronts are rich in harmonics that couple readily to adjacent circuits. *In the design of MECL 10K and MECL 10H, the rise and fall times have been deliberately slowed. This reduces the affinity for crosstalk without compromising other important performance parameters.*

From the above, it is evident that the MECL logic line is not simply capable of operating at high speed, but has been specifically designed to reduce the problems that are normally associated with high–speed operation.

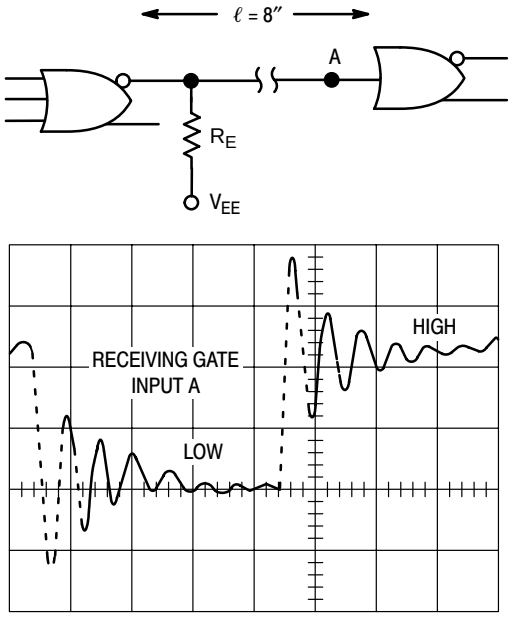


Figure 1. Unterminated Transmission Line (No Ground Plane Used)

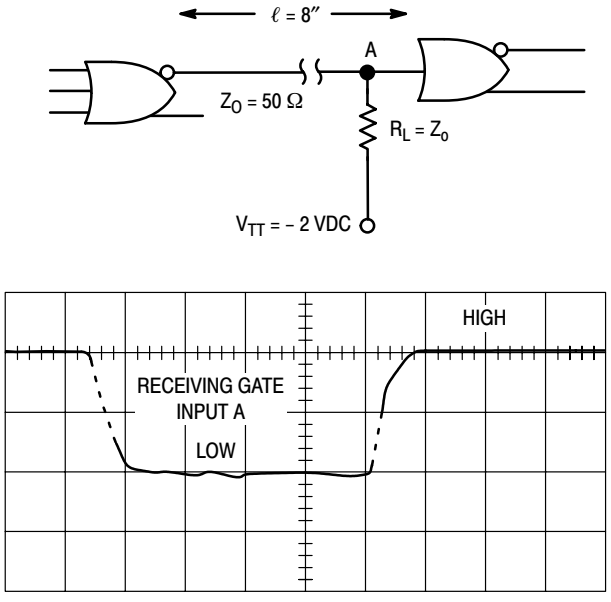


Figure 2. Properly Terminated Transmission Line (Ground Plane Added)

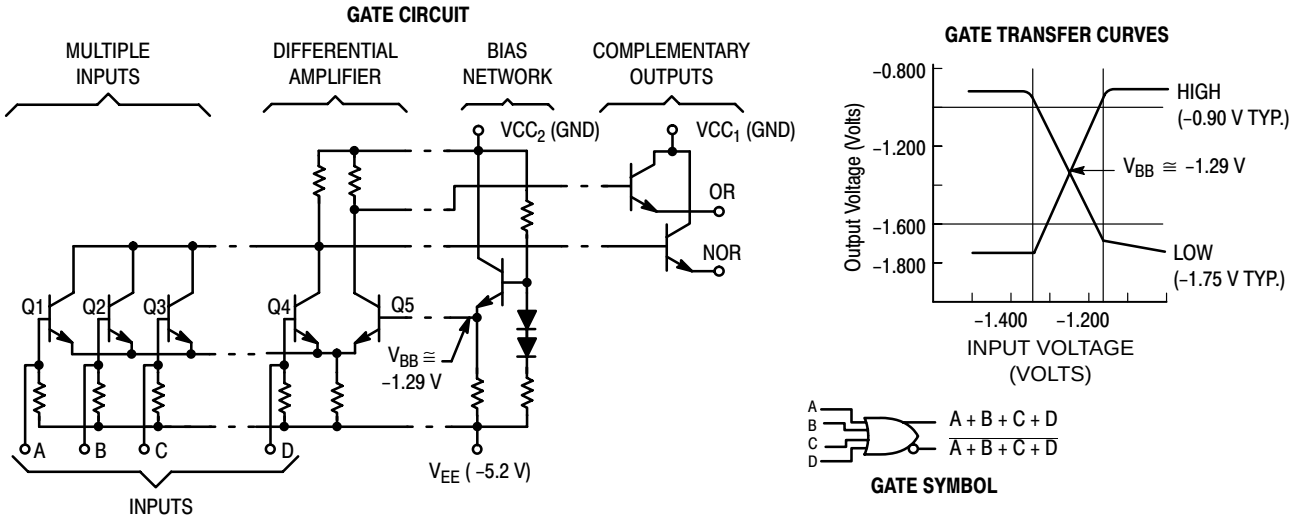


Figure 3. MECL 10K Gate Structure and Switching Behavior

CIRCUIT DESCRIPTION

The typical MECL 10K circuit, Figure 3, consists of a differential–amplifier input circuit, a temperature and voltage compensated bias network, and emitter–follower outputs to restore dc levels and provide buffering for transmission line driving. High fan–out operation is possible because of the high input impedance of the differential amplifier input and the low output impedance of the emitter follower outputs. Power–supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the OR function and its complement, the NOR function. The design of the MECL 10H gate is unchanged, with two exceptions. The bias network has been replaced with a voltage regulator, and the differential amplifier source resistor has been replaced with a constant current source. (See Technical Data section on page 12 for additional MECL 10H information.)

Power–Supply Connections – Any of the power supply levels, V_{TT}, V_{CC}, or V_{EE} may be used as ground; however, the use of the V_{CC} node as ground results in best noise immunity. In such a case: V_{CC} = 0, V_{TT} = –2.0 V, V_{EE} = –5.2 V.

System Logic Specifications – The output logic swing of 0.85 V, as shown by the typical transfer characteristics curve, varies from a LOW state of V_{OL} = –1.75 V to a HIGH state of V_{OH} = –0.9 V with respect to ground.

Positive logic is used when reference is made to logical “0’s” or “1’s.” Then

“0” = –1.75 V = LOW

typical

“1” = –0.9 V = HIGH

Circuit Operation – Beginning with all logic inputs LOW (nominal –1.75 V), assume that Q1 through Q4 are cut off because their P–N base–emitter junctions are not conducting, and the forward–biased Q5 is conducting. Under these conditions, with the base of Q5 held at –1.29 V by the V_{BB} network, its emitter will be one diode drop (0.8 V) more negative than its base, or –2.09 V. (The 0.8 V differential is a characteristic of this P–N junction.) The base–to–emitter differential across Q1 – Q4 is then the difference between the common emitter voltage (–2.09 V) and the LOW logic level (–1.75 V) or 0.34 V. This is less than the threshold voltage of Q1 through Q4 so that these transistors will remain cut off.

When any one (or all) of the logic inputs are shifted upward from the –1.75 V LOW state to the –0.9 V HIGH state, the base voltage of that transistor increases beyond the threshold point and the transistor turns on. When this happens, the voltage at the common–emitter point rises from –2.09 V to –1.7 (one diode drop below the –0.9 V base voltage of the input transistor), and since the base voltage of the fixed–bias transistor (Q5) is held at –1.29 V, the base–emitter voltage Q5 cannot sustain conduction. Hence, this transistor is cut off.

This action is reversible, so that when the input signal(s) return to the LOW state, Q1 – Q4 are again turned off and Q5 again becomes forward biased. The collector voltages resulting from the switching action of Q1 – Q4 and Q5 are transferred through the output emitter–follower to the output terminal. Note that the differential action of the switching transistors (one section being off when the other is on) furnishes simultaneous complementary signals at the output. This action also maintains constant power supply current drain.

DEFINITIONS OF LETTER SYMBOLS AND ABBREVIATIONS

Current:

I_{CC}	Total power supply current drawn from the positive supply by a MECL unit under test.
I_{CBO}	Leakage current from input transistor on MECL devices without pulldown resistors when test voltage is applied.
I_{CCH}	Current drain from V_{CC} power supply with all inputs at logic HIGH level.
I_{CCL}	Current drain from V_{CC} power supply with all inputs at logic LOW level.
I_E	Total power supply current drawn from a MECL test unit by the negative power supply.
I_F	Forward diode current drawn from an input of a saturated logic–to–MECL translator when that input is at 0.4 V.
I_{in}	Current into the input of the test unit when a maximum logic HIGH ($V_{IH\ max}$) is applied at that input.
I_{INH}	HIGH level input current into a node with a specified HIGH level ($V_{IH\ max}$) logic voltage applied to that node. (Same as I_{in} for positive logic.)
I_{INL}	LOW level input current, into a node with a specified LOW level ($V_{IL\ min}$) logic voltage applied to that node.
I_L	Load current that is drawn from a MECL circuit output when measuring the output HIGH level voltage.
I_{OH}	HIGH level output current: the current flowing into the output, at a specified HIGH level output voltage.
I_{OL}	LOW level output current: the current flowing into the output, at a specified LOW level output voltage.
I_{OS}	Output short circuit current.
I_{out}	Output current (from a device or circuit, under such conditions mentioned in context).
I_{OZL}	Output off current LOW – The current flowing out of a disabled 3–state output with a specified LOW output voltage applied.
I_{OZH}	Output off current HIGH – The current flowing into a disabled 3–state output with a specified HIGH output.
I_R	Reverse current drawn from a transistor input of a test unit when V_{EE} is applied to that input.
I_R'	Reverse current leakage into an input of a saturated logic MECL/PECL translator when that input is at V_{CC}.
I_{SC}	Short–circuit current drawn from a translator saturating output when that output is at ground potential.

Voltage:

V_{BB}	Reference bias supply voltage.
V_{BE}	Base–to–emitter voltage drop of a transistor at specified collector and base currents.
V_{CB}	Collector–to–base voltage drop of a transistor at specified collector and base currents.
V_{CC}	General term for the most positive power supply voltage to a MECL device (usually ground, except for translator and interface circuits).
V_{CC1}	Most positive power supply voltage (output devices). (Usually ground for MECL devices.)
V_{CC2}	Most positive power supply voltage (current switches and bias driver). (Usually ground for MECL devices.)
V_{CMR}	The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1.0 V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –5.2 V. Note for PECL operation, the V_{CMR}(min) will be fixed at 5.0 V – $\|V_{CMR}(min)\|$.
V_{EE}	Most negative power supply voltage for a circuit (usually –5.2 V for MECL devices).
V_F	Input voltage for measuring I_F on TTL interface circuits.
V_{IH}	Input logic HIGH voltage level (nominal value).
$V_{IH\ max}$	Maximum HIGH level input voltage: The most positive (least negative) value of high–level input voltage, for which operation of the logic element within specification limits is guaranteed.
V_{IHA}	Input logic HIGH threshold voltage level.
$V_{IHA\ min}$	Minimum input logic HIGH level (threshold) voltage for which performance is specified.
$V_{IH\ min}$	Minimum HIGH level input voltage: The least positive (most negative) value of HIGH level input voltage for which operation of the logic element within specification limits is guaranteed.
V_{IL}	Input logic LOW voltage level (nominal value).
$V_{IL\ max}$	Maximum LOW level input voltage: The most positive (least negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.
V_{ILA}	Input logic LOW threshold voltage level.
$V_{ILA\ max}$	Maximum input logic LOW level (threshold) voltage for which performance is specified.
$V_{IL\ min}$	Minimum LOW level input voltage: The least positive (most negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.

DEFINITIONS OF LETTER SYMBOLS AND ABBREVIATIONS (continued)

Voltage (continued):

t_{AA}	Address Access Time
V_{in}	Input voltage (to a circuit or device).
V_{max}	Maximum (most positive) supply voltage, permitted under a specified set of conditions.
V_{OH}	Output logic HIGH voltage level: The voltage level at an output terminal for a specified output current, with the specified conditions applied to establish a HIGH level at the output.
V_{OHA}	Output logic HIGH threshold voltage level.
$V_{OHA\ min}$	Minimum output HIGH threshold voltage level for which performance is specified.
$V_{OH\ max}$	Maximum output HIGH or high–level voltage for given inputs.
$V_{OH\ min}$	Minimum output HIGH or high–level voltage for given inputs.
V_{OL}	Output logic LOW voltage level: The voltage level at the output terminal for a specified output current, with the specified conditions applied to establish a LOW level at the output.
V_{OLA}	Output logic LOW threshold voltage level.
$V_{OLA\ max}$	Maximum output LOW threshold voltage level for which performance is specified.
$V_{OL\ max}$	Maximum output LOW level voltage for given inputs.
$V_{OL\ min}$	Minimum output LOW level voltage for given inputs.
V_{TT}	Line load–resistor terminating voltage for outputs from a MECL device.

Time Parameters:

t+	Waveform rise time (LOW to HIGH), 10% to 90%, or 20% to 80%, as specified.
t–	Waveform fall time (HIGH to LOW), 90% to 10%, or 80% to 20%, as specified.
t_r	Same as t+.
t_f	Same as t–.
t+–	Propagation Delay, see Figure 9 on page 15.
t–+	Propagation Delay, see Figure 9 on page 15.
t_{pd}	Propagation delay, input to output from the 50% point of the input waveform at pin x (falling edge noted by – or rising edge noted by +) to the 50% point of the output waveform at pin y (falling edge noted by – or rising edge noted by +). (Cf Figure 9 on page 15.)
$t_{x\pm y\pm}$	
t_{x+}	Output waveform rise time as measured from 10% to 90% or 20% to 80% points on waveform (whichever is specified) at pin x with input conditions as specified.
t_{x-}	Output waveform fall time as measured from 90% to 10% or 80% to 20% points on waveform (whichever is specified) at pin x, with input conditions as specified.
f_{Tog}	Toggle frequency of a flip–flop or counter device.
f_{shift}	Shift rate for a shift register.

Temperature:

T_{stg}	Maximum temperature at which device may be stored without damage or performance degradation.
T_J	Junction (or die) temperature of an integrated circuit device.
T_A	Ambient (environment) temperature existing in the immediate vicinity of an integrated circuit device package.
θ_{JA}	Thermal resistance of an IC package, junction to ambient.
θ_{JC}	Thermal resistance of an IC package, junction to case.
lfpm	Linear feet per minute.
θ_{CA}	Thermal resistance of an IC package, case to ambient.

Miscellaneous:

e_g	Signal generator inputs to a test circuit.
TP_{in}	Test point at input of unit under test.
TP_{out}	Test point at output of unit under test.
D.U.T.	Device under test.
C_{in}	Input capacitance.
C_{out}	Output capacitance.
Z_{out}	Output impedance.
P_D	The total DC power applied to a device, not including any power delivered from the device to a load.
R_L	Load Resistance.
R_T	Terminating (load) resistor.
R_p	An input pull–down resistor (i.e., connected to the most negative voltage).
P.U.T.	Pin under test.

MECL LOGIC SURFACE MOUNT

WHY SURFACE MOUNT?

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the State-of-the-Art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and offer increased functions with the same size product.

MECL AVAILABILITY IN SURFACE MOUNT

ON Semiconductor is now offering MECL 10K and MECL 10H in the PLCC (Plastic Leaded Chip Carrier) packages.

MECL in PLCC may be ordered in conventional plastic rails or on Tape and Reel. Refer to the Tape and Reel section for ordering details.

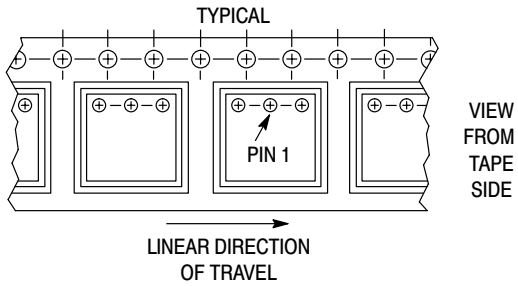
TAPE AND REEL

ON Semiconductor has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. The packaging fully conforms to the latest EIA RS-481A specification. The antistatic embossed tape provides a secure cavity sealed with a peel-back cover tape.

GENERAL INFORMATION

- Reel Size 13 inch (330 mm) Suffix: R2
- Tape Width 16 mm
- Units/Reel 1000

MECHANICAL POLARIZATION



ORDERING INFORMATION

- Minimum Lot Size/Device Type = 3000 Pieces.
- No Partial Reel Counts Available.
- To order devices which are to be delivered in Tape and Reel, add the appropriate suffix to the device number being ordered.

Example:

ORDERING CODE	SHIPMENT METHOD
MC10101FN	Rails
MC10101FNR2	13 inch Tape and Reel
MC10H101FN	Rails
MC10H101FNR2	13 inch Tape and Reel
MC12015D	Rails
MC12015DR2	13 inch Tape and Reel

DUAL-IN-LINE PACKAGE TO PLCC PIN CONVERSION DATA

The following tables give the equivalent I/O pinouts of Dual-In-Line (DIL) packages and Plastic Leaded Chip Carrier (PLCC) packages.

PIN CONVERSION TABLES

8–Pin DIL to 20–Pin PLCC

8 PIN DIL	1	2	3	4	5	6	7	8
20 PIN PLCC	2	5	7	10	12	15	17	20

14–Pin DIL to 20–Pin PLCC

14 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14
20 PIN PLCC	2	3	4	6	8	9	10	12	13	14	16	18	19	20

16–Pin DIL to 20–Pin PLCC

16 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
20 PIN PLCC	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

20–Pin DIL to 20–Pin PLCC

20 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
20 PIN PLCC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

24–Pin DIL to 28–Pin PLCC

24 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
28 PIN PLCC	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28

MECL POSITIVE AND NEGATIVE LOGIC

INTRODUCTION

The increasing popularity and use of emitter coupled logic has created a dilemma for some logic designers. Saturated logic families such as TTL have traditionally been designed with the NAND function as the basic logic function, however, the basic ECL logic function is the NOR function (positive logic). Therefore, the designer may either design ECL systems with positive logic using the NOR, or design with negative logic using the NAND. Which is the more convenient? On the one hand the designer is familiar with positive logic levels and definitions, and on the other hand, he is familiar with implementing systems using NAND functions. Perhaps a presentation of the basic definitions and characteristics of positive and negative logic will clarify the situation and eliminate misunderstanding.

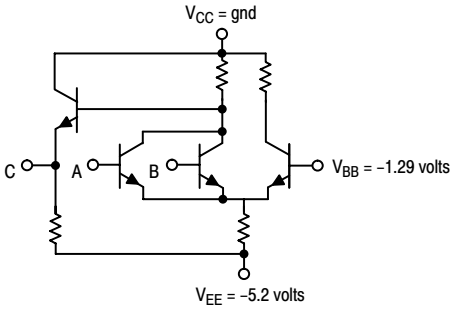


Table 3.

INPUTS		OUTPUT
A	B	C
LO	LO	HI
LO	HI	LO
HI	LO	LO
HI	HI	LO

HI = −0.9 volts
LO = −1.7 volts

Table 4.

NEGATIVE LOGIC

INPUTS		OUTPUT
A	B	C
1	1	0
1	0	1
0	1	1
0	0	1

$C = \overline{A \bullet B}$

Table 5.

POSITIVE LOGIC

INPUTS		OUTPUT
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

$C = \overline{A + B}$

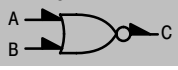


Figure 4. Basic MECL Gate Circuit and Logic Function in Positive and Negative Nomenclature

LOGIC EQUIVALENCIES

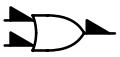
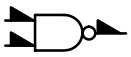
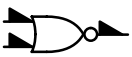
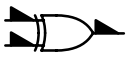
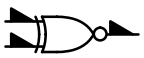
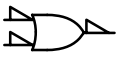
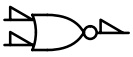
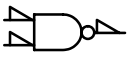
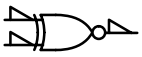
Binary logic must have two states to represent the binary 1 and 0. With ECL the typical states are a high level of –0.9 volts and a low level of –1.7 volts. Two choices are possible then to represent the binary 1 and 0. Positive logic defines the 1 or “true” state as the most positive voltage level, whereas negative logic defines the most negative voltage level as the 1 or “true” state. Because of the difference in definition of states, the basic ECL gate is a NOR function in positive logic and is a NAND function in negative logic.

Figure 4 more clearly shows the above comparison of functions. Table 3 lists the output voltage level as a function of input voltage levels of the MECL gate circuit shown. Table 4 translates the voltage levels into the appropriate negative logic levels which show the function to be $C = \overline{A \bullet B}$; that is, the circuit performs the NAND function. Table 5 translates the equivalent positive logic function into $C = \overline{A + B}$, the NOR function.

Similar comparisons could be made for other positive logic functions. As an example, the positive OR function translates to the negative AND function. Table 6 shows a comparison of several common logic functions.

Any function available in a logic family may be expressed in terms of positive or negative logic, bearing in mind the definition of logic levels. The choice of logic definition, as previously stated, is dependent on the designer. ON Semiconductor provides both positive and negative logic symbols on data sheets for the popular MECL 10,000 logic series.

Table 6. Comparative Positive and Negative Logic Functions

		POSITIVE LOGIC					
INPUTS							
A	B	AND	OR	NAND	NOR	EXOR	EXNOR
LO	LO	LO	LO	HI	HI	LO	HI
LO	HI	LO	HI	HI	LO	HI	LO
HI	LO	LO	HI	HI	LO	HI	LO
HI	HI	HI	HI	LO	LO	LO	HI
A	B	OR	AND	NOR	NAND	EXNOR	EXOR
INPUTS							
		NEGATIVE LOGIC					

SUMMARY

Conversion from one logic form to another or the use of a particular logic form need not be a complicated process. If the designer uses the logic form with which he is familiar and bears in mind the previously mentioned definition of levels, problems arising from definition of logic functions should be minimized.

REFERENCE

Y. Chu, Digital Computer Design Fundamentals
New York, McGraw–Hill, 1962.

TECHNICAL DATA

GENERAL CHARACTERISTICS AND SPECIFICATIONS

In subsequent sections of this document, the important MECL parameters are identified and characterized, and complete data provided for each of the functions. To make this data as useful as possible, and to avoid a great deal of repetition, the data that is common to all functional blocks in a line is not repeated on each individual sheet. Rather, these common characteristics, as well as the application information that applies to each family, are discussed.

In general, the common characteristics of major importance are:

Maximum Ratings, including both DC and AC characteristics and temperature limits;

Transfer Characteristics, which define logic levels and switching thresholds;

DC Parameters, such as output levels, threshold levels, and forcing functions.

AC Parameters, such as propagation delays, rise and fall times and other time dependent characteristics.

In addition, this document will discuss general layout and design guides that will help the designer in building and testing systems with MECL circuits.

MAXIMUM RATINGS

The limit parameters beyond which the life of the devices may be impaired are given in Table 7. In addition, Table 8 provides certain limits which, if exceeded, will not damage the devices, but could degrade the performance below that of the guaranteed specifications.

Table 7. Limits Beyond which Device Life may be Impaired

Characteristic	Symbol	Unit	MECL 10H	MECL 10K
Power Supply	V_{EE}	Vdc	–8.0 to 0	–8.0 to 0
Input Voltage (V_{CC} = 0)	V_{in}	Vdc	0 to V_{EE}	0 to V_{EE}
Output Source Current Continuous	I_{out}	mAdc	50	50
Output Source Current Surge	I_{out}	mAdc	100	100
Storage Temperature	T_{stg}	°C	–65 to +150	–65 to +150
Junction Temperature Ceramic Package (Note 1)	T_J	°C	165	165
Junction Temperature Plastic Package (Note 2)	T_J	°C	140	140

1. Maximum T_J may be exceeded ($\leq$ 250°C) for short periods of time ($\leq$ 240 hours) without significant reduction in device life.
2. For long term ($\geq$ 10 yrs.) max T_J of 110°C required. Max T_J may be exceeded ($\leq$ 175°C) for short periods of time ($\leq$ 240 hours) without significant reduction in device life.

Table 8. Limits Beyond which Performance may be Degraded

Characteristic	Symbol	Unit	MECL 10H	MECL 10K
Operating Temperature Range Commercial (Note 3)	T_A	°C	0 to +75	–30 to +85
Supply Voltage (V_{CC} = 0)	V_{EE}	Vdc	–4.94 to –5.46	–4.68 to –5.72 (Note 4)
Output Drive Commercial	–	Ω	50 Ω to –2.0 Vdc	50 Ω to –2.0 Vdc

3. With airflow $\geq$ 500 lfpm.
4. Functionality only. Data sheet limits are specified for –5.2 V ± 0.010 V.
5. Except MC1648 which has an internal output pulldown resistor.

MECL TRANSFER CURVES and SPECIFICATION TEST POINTS

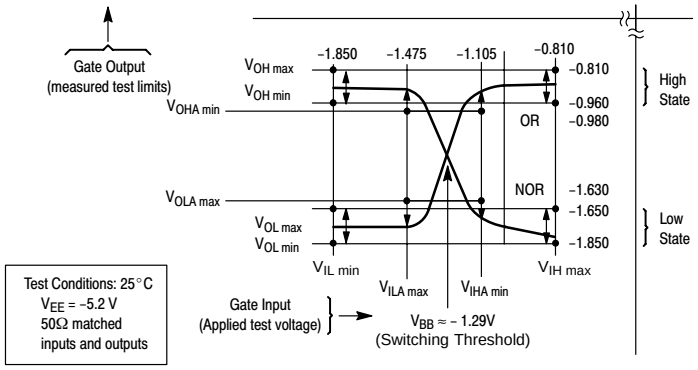


Figure 5. MECL 10K

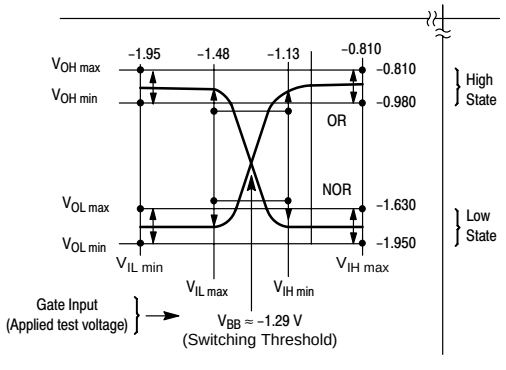


Figure 6. MECL 10H

MECL TRANSFER CURVES

For MECL logic gates, the dual (complementary) outputs must be represented by two transfer curves: one to describe the OR switching action and one to describe the NOR switching action. Typical transfer curves and associated data for the MECL 10K/10H family are shown in Figure 5 and Figure 6, respectively.

It is not necessary to measure transfer curves at all points of the curves. To guarantee correct operation it is sufficient merely to measure two sets of min/max logic level parameters.

The first set is obtained for 10K by applying test voltages, $V_{IL\ min}$ and $V_{IH\ max}$ (sequentially) to the gate inputs, and measuring the OR and NOR output levels to make sure they are between $V_{OL\ max}$ and $V_{OL\ min}$, and $V_{OH\ max}$ and $V_{OH\ min}$ specifications.

The second set of logic level parameters relates to the switching thresholds. This set of data is distinguished by an "A" in symbol subscripts. A test voltage, $V_{ILA\ max}$, is applied to the gate and the NOR and OR outputs are measured to see that they are above the $V_{OHA\ min}$ and below the $V_{OLA\ max}$ levels, respectively. Similar checks are made using the test input voltage $V_{IHA\ min}$.

The result of these specifications insures that:

a . The switching threshold ($\approx V_{BB}$) falls within the darkest rectangle; i.e. switching does not begin outside this rectangle;

b . Quiescent logic levels fall in the lightest shaded ranges;

c . Guaranteed noise immunity is met.

As shown in Figure 7, MECL 10K outputs rise with increasing ambient temperature. All circuits in each family have the same worst–case output level specifications regardless of power dissipation or junction temperature differences to reduce loss of noise margin due to thermal differences.

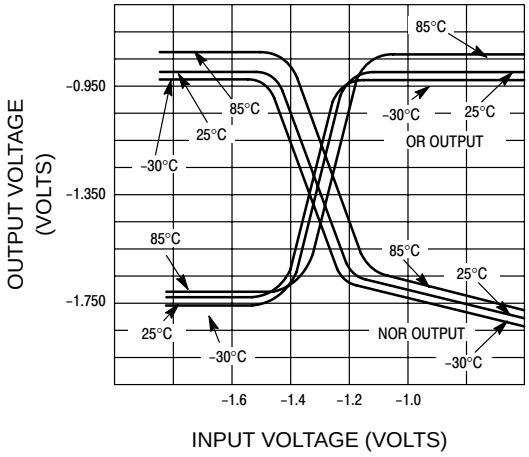


Figure 7. Typical Transfer Characteristics as a Function of Temperature (MECL 10K)

All of these specifications assume –5.2 V power supply operation. Operation at other power–supply voltages is possible, but will result in further transfer curve changes. Table 9 gives rate of change of output voltages as a function of power supply.

Table 9. Typical Level Change Rates/1.0 V

Voltage	MECL 10H	MECL 10K
$\Delta V_{OH}/\Delta V_{EE}$	0.008	0.016
$\Delta V_{OL}/\Delta V_{EE}$	0.020	0.250
$\Delta V_{BB}/\Delta V_{EE}$	0.010	0.148

NOISE MARGIN

"Noise margin" is a measure of logic circuit's resistance to undesired switching. MECL noise margin is defined in terms of the specification points surrounding the switching threshold. The critical parameters of interest here are those designated with the "A" subscript ($V_{OHA\ min}$, $V_{OLA\ max}$, $V_{IHA\ min}$, $V_{ILA\ max}$) in the transfer characteristic curves. MECL 10H is specified and tested with:

$V_{OHA\ min} = V_{OH\ min}$

$V_{OLA\ max} = V_{OL\ max}$

$V_{IHA\ min} = V_{IH\ min}$

and

$V_{ILA\ max} = V_{IL\ max}$

Guaranteed noise margin (NM) is defined as follows:

$NM_{HIGH\ LEVEL} = V_{OHA\ min} - V_{IHA\ min}$

$NM_{LOW\ LEVEL} = V_{ILA\ max} - V_{OLA\ max}$

To see how noise margin is computed, assume a MECL gate drives a similar MECL gate, Figure 8.

At a gate input (point B) equal to $V_{ILA\ max}$, MECL gate #2 can begin to enter the shaded transition region.

This is a "worst case" condition, since the $V_{OLA\ max}$ specification point guarantees that no device can enter the transition region before an input equal to $V_{ILA\ max}$ is reached. Clearly then, $V_{ILA\ max}$ is one critical point for noise margin computation, since it is the edge of the transition region.

To find the other critical voltage, consider the output from MECL gate #1 (point A). What is the most positive value possible for this voltage (considering worst case specifications)? From Figure 8 it can be observed that the $V_{OLA\ max}$ specification insures that the LOW state OR output from gate #1 can be no greater than $V_{OLA\ max}$.

Note that $V_{OLA\ max}$ is more negative than $V_{ILA\ max}$. Thus, with $V_{OLA\ max}$ at the input to gate #2, the transition region is not yet reached. (The input voltage to gate #2 is still to the left of $V_{ILA\ max}$ on the transfer curve.)

In order to ever run the chance of switching gate #2, we would need an additional voltage, to move the input from $V_{OLA\ max}$ to $V_{ILA\ max}$. This constitutes the "safety factor" known as noise margin. It can be calculated as the magnitude of the difference between the two specification voltages, or for the MECL 10K levels shown:

$$NM_{LOW} = -V_{ILA\ max} - V_{OLA\ max}$$
$$= -(-1.475\ V) - (-1.630\ V)$$
$$= 155\ mV.$$

Similarly, for the HIGH state:

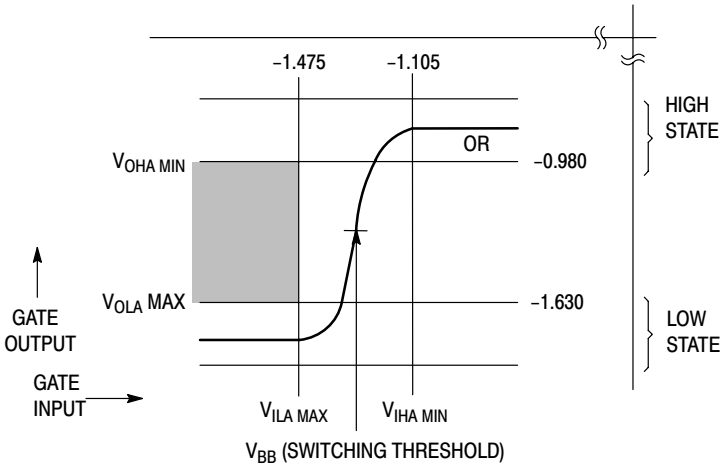
$$NM_{HIGH} = -V_{OHA\ min} - V_{IHA\ min}$$
$$= -(-0.980\ V) - (-1.105\ V)$$
$$= 125\ mV$$

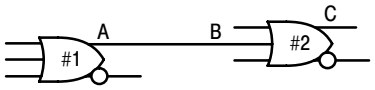
Analogous results are obtained when considering the "NOR" transfer data.

Note that these noise margins are absolute worst case conditions. The lessor of the two noise margins is that for the HIGH state, 125 mV. This then, constitutes the guaranteed margin against signal undershoot, and power or thermal disturbances.

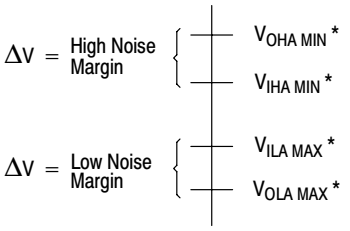
As shown in the table, typical noise margins are usually better than guaranteed – by about 75 mV. For MECL 10H the "noise margin" is 150 mV for NM low and NM high.

Noise margin is a dc specification that can be calculated, since it is defined by specification points tabulated on MECL data sheets. However, by itself, this specification does not give a complete picture regarding the noise immunity of a system built with a particular set of circuits. Overall system noise immunity involves not only noise–margin specifications, but also other circuit–related factors that determine how difficult it is to apply a noise signal of sufficient magnitude and duration to cause the circuit to propagate a false logic state. In general, then, noise immunity involves line impedances, circuit output impedances, and propagation delay in addition to noise–margin specifications. This subject to discussed in greater detail in the MECL System Design Handbook, HB205/D.





Specification Points for Determining Noise Margin



*$V_{OHA\ min} = V_{OH\ min}$, $V_{OLA\ max} = V_{OL\ max}$, $V_{IHA\ min} = V_{IH\ min}$ and $V_{ILA\ max} = V_{IL\ max}$ for MECL 10H.

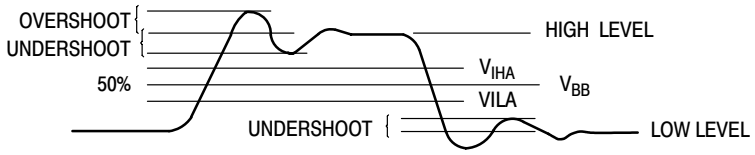
Table 10. Noise Margin Computations

Family	Guaranteed Worst–Case DC Noise Margin (V)	Typical DC Noise Margin (V)
MECL 10H	0.150	0.270
MECL 10K	0.125	0.210

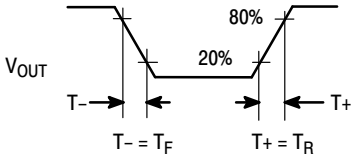
Figure 8. MECL Noise Margin Data

AC OR SWITCHING PARAMETERS

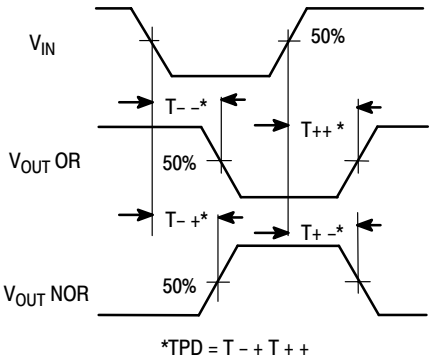
Time–dependent specifications are those that define the effects of the circuit on a specified input signal, as it travels through the circuit. They include the time delay involved in changing the output level from one logic state to another. In addition, they include the time required for the output of a circuit to respond to the input signal, designated as propagation delay, MECL waveform and propagation delay terminologies are depicted in Figure 9. Specific rise, fall, and propagation delay times are given on the data sheet for each specific functional block, but like the transfer characteristics, ac parameters are temperature and voltage dependent. Typical variations for MECL 10K are given in the curves of Figures 10 through 13.



MECL WAVEFORM TERMINOLOGY



MECL 10K and MECL 10H Rise and Fall Times



MECL Propagation Delay

Figure 9. Typical Logic Waveforms

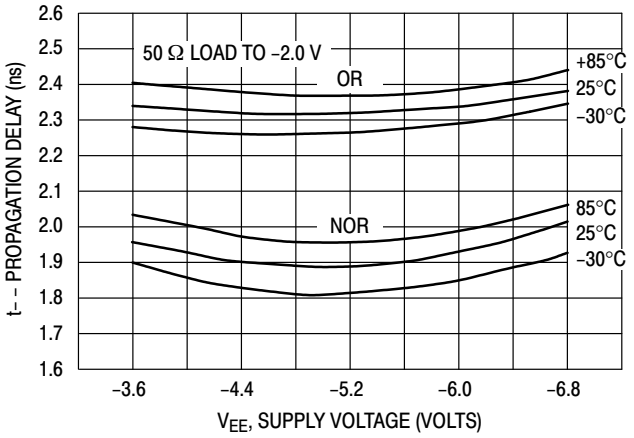


Figure 10. Typical Propagation Delay t– – vs. V_{EE} and Temperature (MECL 10K)

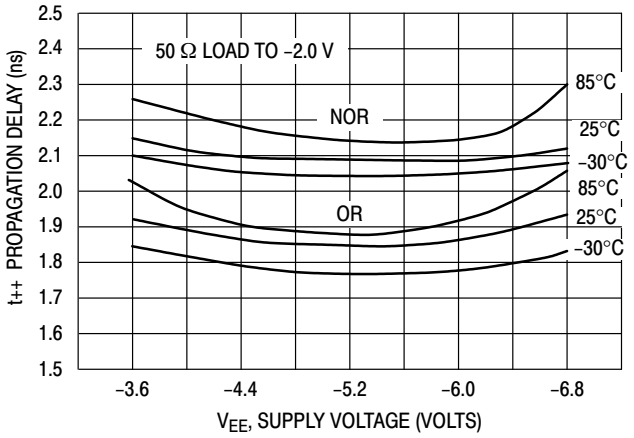


Figure 11. Typical Propagation Delay t++ vs. V_{EE} and Temperature (MECL 10K)

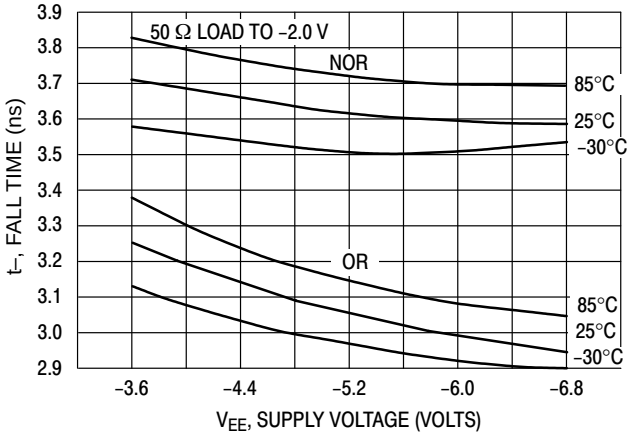


Figure 12. Typical Fall Time (90% to 10%) vs. Temperature and Supply Voltage (MECL 10K)

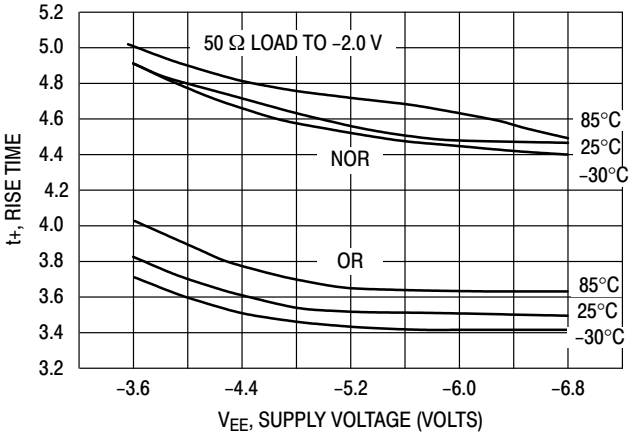


Figure 13. Typical Fall Time (10% to 90%) vs. Temperature and Supply Voltage (MECL 10K)

SETUP AND HOLD TIMES

Setup and hold times are two AC parameters which can easily be confused unless clearly defined. For MECL logic devices, t_{setup} is the minimum time (50% – 50%) before the positive transition of the clock pulse (C) that information must be present at the Data input (D) to insure proper operation of the device. The t_{hold} is defined similarly as the minimum time after the positive transition of the clock pulse (C) that the information must remain unchanged at the Data input (D) to insure proper operation. Setup and hold waveforms for logic devices are shown in Figure 14.

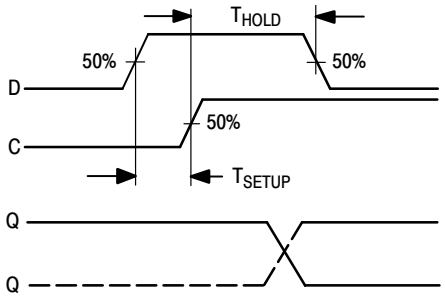


Figure 14. Setup and Hold Waveforms for MECL Logic Devices

TESTING MECL 10H AND MECL 10K

To obtain results correlating with ON Semiconductor circuit specifications certain test techniques must be used. A schematic of a typical gate test circuit is shown in Figure 15. This test circuit is the standard ac test configuration for most MECL devices. (Exceptions are shown with device specification.)

A solid ground plane is used in the test setup, and capacitors bypass V_{CC1}, V_{CC2}, and V_{EE} pins to ground. All power leads and signal leads are kept as short as possible.

The sampling scope interface runs directly to the 50 ohm inputs of Channel A and B via 50 ohm coaxial cable. Equal–length coaxial cables must be used between the test set and the A and B scope inputs. A 50 ohm coax cable such as RG58/U or RG188A/U, is recommended.

Interconnect fittings should be 50 ohm GR, BNC, Sealectro Conhex, or equivalent. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

The pulse generator must be capable of 2.0 ns rise and fall times for MECL 10K and 1.5 ns for MECL 10H and MECL III. In addition, the generator voltage must have an offset to give MECL signal swings of ≈ ±400 mV about a threshold of ≈ +0.7 V when V_{CC} = +2.0 and V_{EE} = –3.2 V for AC testing of logic devices.

The power supplies are shifted +2.0 V, so that the device under test has only one resistor value to load into the precision 50 ohm input impedance of the sampling oscilloscope. Use of this technique yields a close correlation between ON Semiconductor and customer testing. Unused outputs are loaded with a 50 ohm resistor (100 ohm for MC105XX devices) to ground. The positive supply (V_{CC}) should be decoupled from the test board by RF type 25 μF capacitors to ground. The V_{CC} pins are bypassed to ground with 0.1 μF, as is the V_{EE} pin.

Additional information on testing MECL 10K and understanding data sheets is found in Application Note AN701/D and the MECL System Design Handbook, HB205/D.

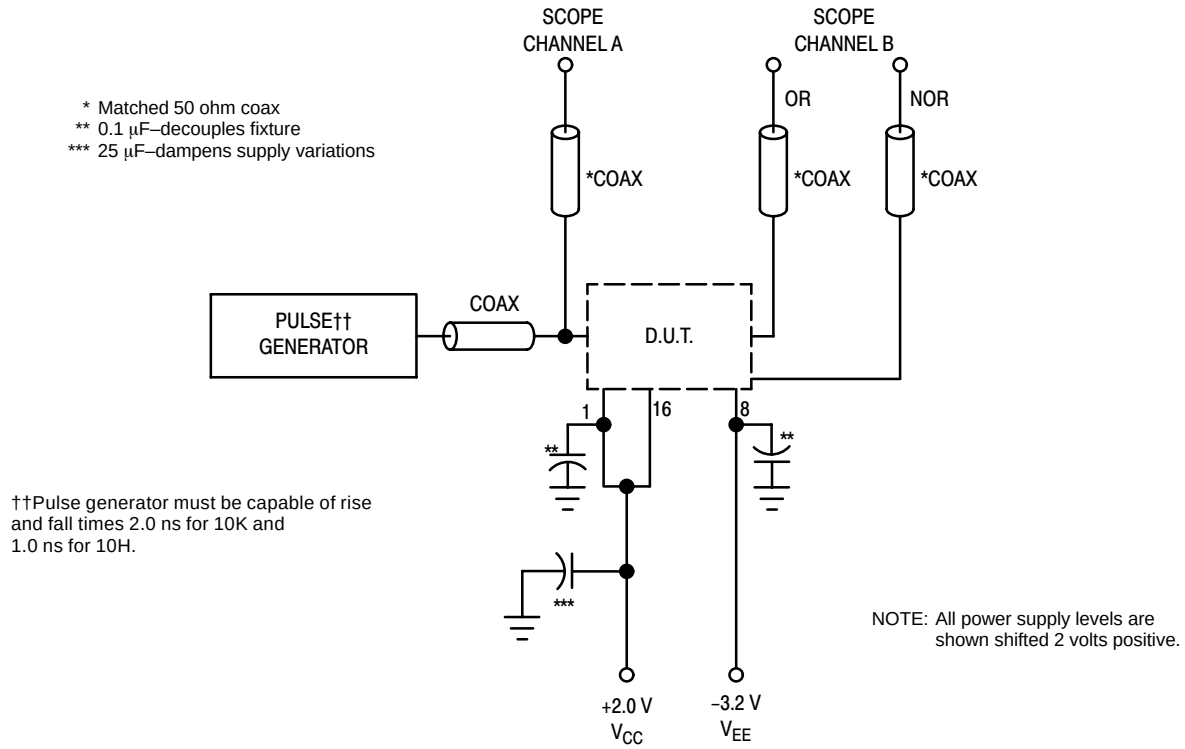


Figure 15. MECL Logic Switching Time Test Setup

OPERATIONAL DATA

POWER SUPPLY CONSIDERATIONS

MECL circuits are characterized with the V_{CC} point at ground potential and the V_{EE} point at –5.2 V. While this MECL convention is not necessarily mandatory, it does result in maximum noise immunity. This is so because any noise induced on the V_{EE} line is applied to the circuit as a common–mode signal which is rejected by the differential action of the MECL input circuit. Noise induced into the V_{CC} line is not cancelled out in this fashion. Hence, a good system ground at the V_{CC} bus is required for best noise immunity. Also, MECL 10H circuits may be operated with V_{EE} at –4.5 V with a negligible loss of noise immunity.

Power supply regulation which will achieve 10% regulation or better at the device level is recommended. The –5.2 V power supply potential will result in best circuit speed. Other values for V_{EE} may be used. A more negative voltage will increase noise margins at a cost of increased power dissipation. A less negative voltage will have just the opposite effect. (Noise margins and performance specifications of MECL 10H are unaffected by variations in V_{EE} because of the internal voltage regulation.)

On logic cards, a ground plane or ground bus system should be used. A bus system should be wide enough to prevent significant voltage drops between supply and device and to produce a low source inductance.

Although little power supply noise is generated by MECL logic, power supply bypass capacitors are recommended to handle switching currents caused by stray capacitance and asymmetric circuit loading. A parallel combination of a 1.0 μF and a 100 pF capacitor at the power entrance to the board, and a 0.01 μF low–inductance capacitor between ground and the –5.2 V line every four to six packages, are recommended.

Most MECL 10H, MECL 10K and MECL III circuits have two V_{CC} leads. V_{CC1} supplies current to the output transistors and V_{CC2} is connected to the circuit logic transistors. The separate V_{CC} pins reduce cross–coupling between individual circuits within a package when the outputs are driving heavy loads. Circuits with large drive capability, similar to the MC10110, have two V_{CC1} pins. All V_{CC} pins should be connected to the ground plane or ground bus as close to the package as possible.

For further discussion of MECL power supply considerations to be made in system designing, see MECL System Design Handbook, HB205/D.

POWER DISSIPATION

The power dissipation of MECL functional blocks is specified on their respective data sheets. This specification does not include power dissipated in the output devices due to output termination. The omission of internal output pulldown resistors permits the use of external terminations designed to yield best system performance. To obtain total operating power dissipation of a particular functional block in a system, the dissipation of the output transistor, under load, must be added to the circuit power dissipation.

Table 11 lists the power dissipation in the output transistors plus that in the external terminating resistors, for the more commonly used termination values and circuit configurations. To obtain true package power dissipation, one output–transistor power–dissipation value must be added to the specified package power dissipation for each external termination resistor used in conjunction with that package. To obtain system power dissipation, the stated dissipation in the external terminating resistors must be added as well. Unused outputs draw no power and may be ignored.

Table 11. Average Power Dissipation in Output Circuit with External Terminating Resistors

Terminating Resistor Value	Output Transistor Power Dissipation (mW)	Terminating Resistor Power Dissipation (mW)
150 ohms to –2.0 Vdc	5.0	4.3
100 ohms to –2.0 Vdc	7.5	6.5
75 ohms to –2.0 Vdc	10	8.7
50 ohms to –2.0 Vdc	15	13
2.0 k ohms to V_{EE}	2.5	7.7
1.0 k ohm to V_{EE}	4.9	15.4
680 ohms to V_{EE}	7.2	22.6
510 ohms to V_{EE}	9.7	30.2
270 ohms to V_{EE}	18.3	57.2
82 ohms to V_{CC} and 130 ohms to V_{EE}	15	140

LOADING CHARACTERISTICS

The differential input to MECL circuits offers several advantages. Its common–mode–rejection feature offers immunity against power–supply noise injection, and its relatively high input impedance makes it possible for any circuit to drive a relatively large number of inputs without deterioration of the guaranteed noise margin. Hence, dc fanout with MECL circuits does not normally present a design problem.

Graphs showing typical output voltage levels as a function of load current for MECL 10H, MECL 10K and MECL III shown in Figure 16. These graphs can be used to determine the actual output voltages for loads exceeding normal operation.

While DC loading causes a change in output voltage levels, thereby tending to affect noise margins, AC loading increases the capacitances associated with the circuit and, therefore, affects circuit speed, primarily rise and fall times.

MECL circuits typically have a 7.0 ohm output impedance and a relatively unaffected by capacitive loading on a positive–going output signal. However, the negative–going edge is dependent on the output pulldown or termination resistor. Loading close to a MECL output pin will cause an additional propagation delay of 0.1 ns per fanout load with a 50 ohm resistor to –2.0 Vdc or 270 ohms to –5.2 Vdc. A 100 ohm resistor to –2.0 Vdc or 510 ohms to –5.2 Vdc results in an additional 0.2 ns propagation delay per fanout load.

Terminated transmission line signal interconnections are used for best system performance. The propagation delay and rise time of a driving gate are affected very little by capacitance loading along a matched parallel–terminated transmission line. However, the delay and characteristic impedance of the transmission line itself are affected by the distributed capacitance. Signal propagation down the line will be increased by a factor, $\sqrt{1 + C_d/C_o}$. Here C_o is the normal intrinsic line capacitance, and C_d is the distributed capacitance due to loading and stubs off the line.

Maximum allowable stub lengths for loading off of a MECL 10K transmission line vary with the line impedance. For example, with Z_o = 50 ohms, maximum stub length would be 4.5 inches (1.8 in. for MECL III). But when Z_o = 100 ohms, the maximum allowable stub length is decreased to 2.8 inches (1.0 in. for MECL III).

The input loading capacitance of a MECL 10H and MECL 10K gate is about 2.9 pF and 3.3 pF for MECL III. To allow for the IC connector or solder connection and a short stub length, 5.0 to 7.0 pF is commonly used in loading calculations.

UNUSED MECL INPUTS

The input impedance of a differential amplifier, as used in the typical MECL input circuit, is very high when the applied signal level is low. Under low–signal conditions, therefore, any leakage to the input capacitance of the gate could cause a gradual buildup of voltage on the input lead, thereby adversely affecting the switching characteristics at low repetition rates.

All single–ended input MECL logic circuits contain input pulldown resistors between the input transistor bases and V_{EE}. As a result, unused inputs may be left unconnected (the resistor provides a sink for I_{CBO} leakage currents, and inputs are held sufficiently negative that circuits will not trigger due to noise coupled into such inputs). Input pulldown resistor values are typically 50 kΩ and are not to be used as pulldown resistors for preceding open–emitter outputs.

Some MECL devices do not have input pulldowns. Examples are the differential line receivers. If a single differential receiver within a package is unused, one input of that receiver must be tied to the V_{BB} pin provided, and the other input goes to V_{EE} or is left open.

MECL circuits do not operate properly when inputs are connected to V_{CC} for a HIGH logic level. Proper design practice is to set a HIGH level about –0.9 volts below V_{CC} with a resistor divider, a diode drop, or an unused gate output.

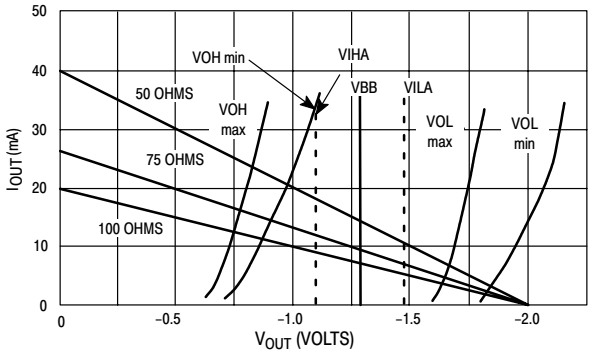


Figure 16. Output Voltage Levels vs. DC Loading (Load Lines for Termination to –2.0 Vdc 25°C)

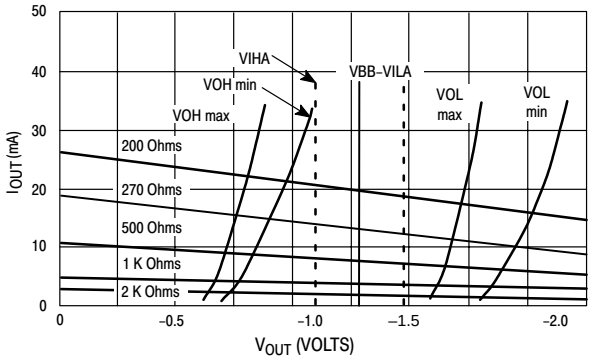


Figure 17. Output Voltage Levels vs. DC Loading (Load Lines for Termination to V_{EE} (–5.2 Vdc) 25°C)

SYSTEM DESIGN CONSIDERATIONS

THERMAL MANAGEMENT

Circuit performance and long–term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit – from the junction region to the ambient environment. The basic formula (a) for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\overline{\theta}_{JC} + \overline{\theta}_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D(\overline{\theta}_{JA}) \quad (2)$$

where

T_J = maximum junction temperature
T_A = maximum ambient temperature
P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation section on page 18).
$\overline{\theta}_{JC}$ = average thermal resistance, junction to case
$\overline{\theta}_{CA}$ = average thermal resistance, case to ambient
$\overline{\theta}_{JA}$ = average thermal resistance, junction to ambient

This ON Semiconductor recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL–M–38510 (JAN) MECL 10K devices.

Only two terms on the right side of equation (1) can be varied by the user – the ambient temperature, and the device case–to–ambient thermal resistance, $\overline{\theta}_{CA}$. (To some extent the device power dissipation can be also controlled, but under recommended use the V_{EE} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\overline{\theta}_{CA}$ thermal resistance term. $\overline{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

Table 12. Thermal Resistance Values for Standard MECL I/D Packages

Thermal Resistance in Still Air										
Package Description							θ_{JA} (°C/Watt)		θ_{JC} (°C/Watt)	
No. Leads	Body Style	Body Material	Body WxL	Die Bond	Die Area (Sq. Mils)	Flag Area (Sq. Mils)	Avg.	Max.	Avg.	Max.
8	DIL	EPOXY	1/4″×3/8″	EPOXY	2496	8100	102	133	50	80
8	DIL	ALUMINA	1/4″×3/8″	SILVER/GLASS	2496	N/A	140	182	35	56
14	DIL	EPOXY	1/4″×3/4″	EPOXY	4096	6400	84	109	38	61
14	DIL	ALUMINA	1/4″×3/4″	SILVER/GLASS	4096	N/A	100	130	25	40
16	DIL	EPOXY	1/4″×3/4″	EPOXY	4096	12100	70	91	34	54
16	DIL	ALUMINA	1/4″×3/4″	SILVER/GLASS	4096	N/A	100	130	25	40
20	PLCC	EPOXY	0.35″×0.35″	EPOXY	4096	14,400	74	82	N/A (Note 11)	N/A (Note 11)
24	DIL (4)	EPOXY	1/2″×1–1/4″	EPOXY	8192	22500	67	87	31	50
24	DIL (5)	ALUMINA	1/2″×1–1/4″	SILVER/GLASS	8192	N/A	50	65	10	16
28	PLCC	EPOXY	0.45″×0.45″	EPOXY	7134	28,900	65	68	N/A (Note 11)	N/A (Note 11)

6. All plastic packages use copper lead frames – ceramic packages use alloy 42 frames.
7. Body style DIL is "Dual–In–Line."
8. Standard Mounting Methods:
   a. Dual–In–Line In Socket or P/C board with no contact between bottom of package and socket or P/C board.
   b. PLCC packages solder attached to traces on 2.24″ × 2.24″ × 0.062″ FR4 type glass epoxy board with 1 oz./S.F. copper (solder coated) mounted to tester with 3 leads of 24 gauge copper wire.
9. Case Outline 649.
10. Case Outline 623.
11. $\theta_{JC} = \theta_{JA} - \left(\frac{T_C - T_A}{P_D}\right)$

    T_C = Case Temperature (determined by thermocouple).

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature–controlled heatsink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D (\overline{\theta}_{JC}) \quad (3)$$

where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average thermal resistance values for standard MECL IC packages are given in Table 12. In , this basic data is converted into graphs showing the maximum power dissipation allowable at various ambient temperatures (still air) for circuits mounted in the different packages, taking into account the maximum permissible operating junction temperature for long term life ($\geqslant$ 100,000 hours for ceramic packages).

AIR FLOW

The effect of air flow over the packages on $\overline{\theta}_{JA}$ (due to a decrease in $\overline{\theta}_{CA}$) is illustrated in the graphs of Figures 18 through 20. This air flow reduces the thermal resistance of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

As an example of the use of the information above, the maximum junction temperature for a 16 lead ceramic dual–in–line packaged MECL 10K quad OR/NOR gate (MC10101L) loaded with four 50 ohm loads can be calculated. Maximum total power dissipation (including 4 output loads) for this quad gate is 195 mW. Assume for this thermal study that air flow is 500 linear feet per minute. From Figure 21, $\overline{\theta}_{JA}$ is 50°C/W. With T_A (air flow temperature at the device) equal to 25°C, the following maximum junction temperature results:

$$T_J = P_D (\overline{\theta}_{JA}) + T_A$$
$$T_J = (0.195\ W)\ (50°C/W) + 25°C = 34.8°C$$

Under the above operating conditions, the MECL 10K quad gate has its junction elevated above ambient temperature by only 9.8°C.

Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperatures as the air passes over the devices, or differences in ambient temperature between two devices.

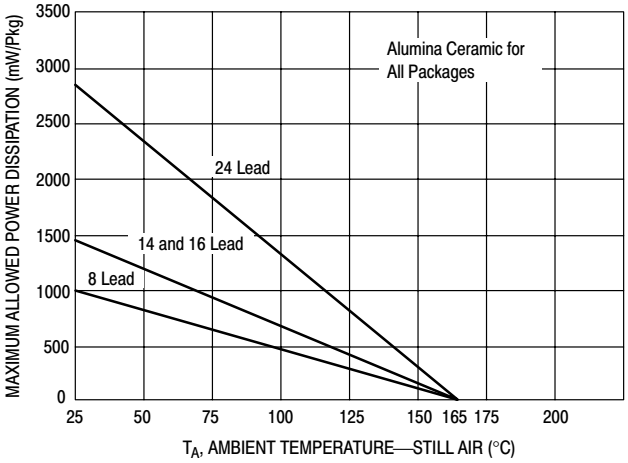


Figure 18. Ambient Temperature Derating Curves (Ceramic Dual–In–Line Package)

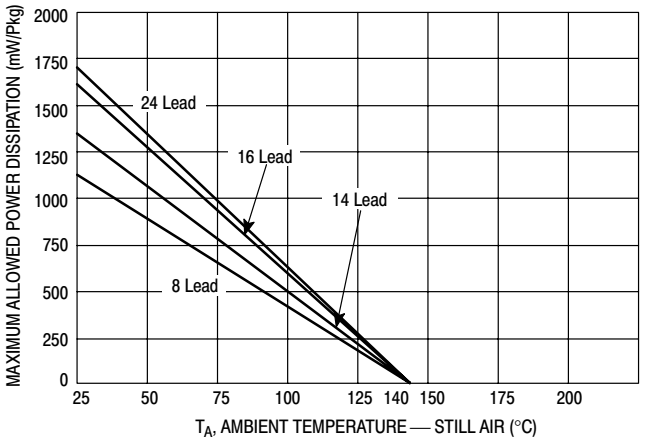


Figure 19. Ambient Temperature Derating Curves (Plastic Dual–In–Line Package)

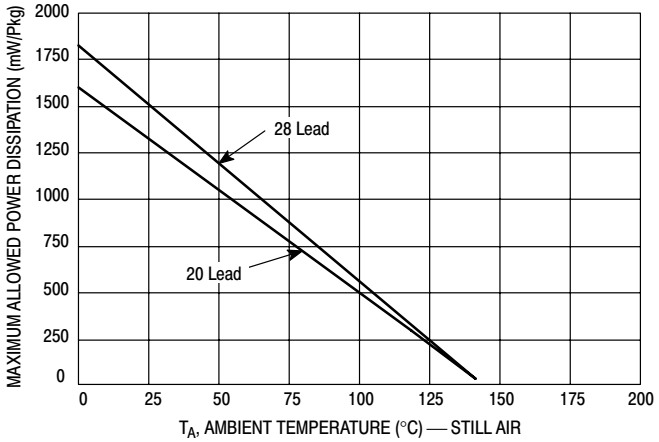


Figure 20. Ambient Temperature Derating Curves (PLCC Package)

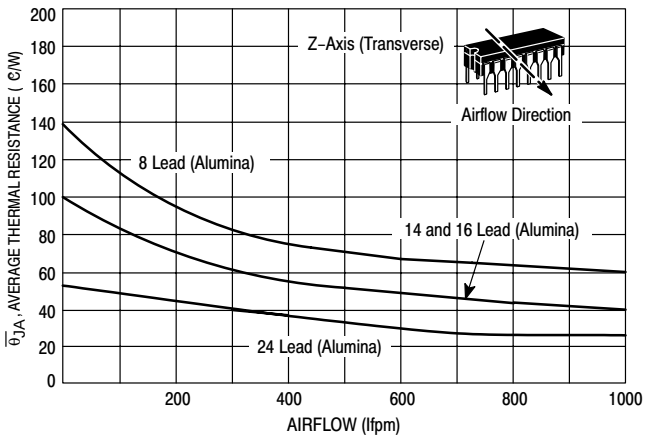


Figure 21. Airflow vs. Thermal Resistance (Ceramic Dual–In–Line Package)

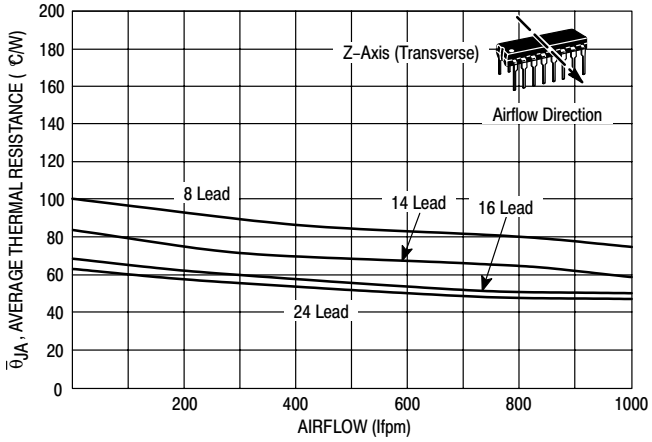


Figure 22. Airflow vs. Thermal Resistance (Plastic Dual–In–Line Package)

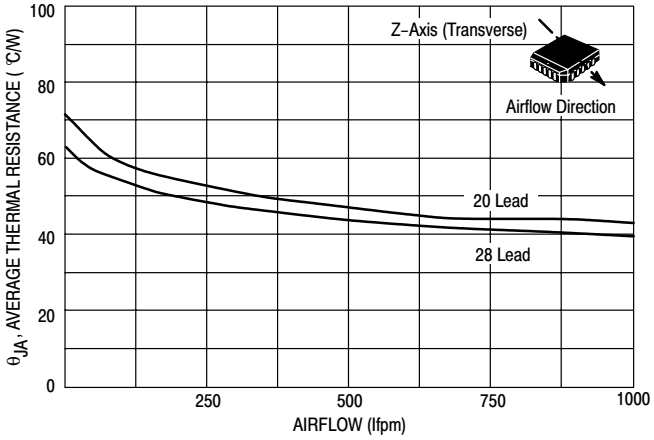


Figure 23. Airflow vs. Thermal Resistance (PLCC Package)

Table 13. Thermal Gradient of Junction Temperature (16–Pin MECL Dual–In–Line Package)

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062″ PC board with Z axis spacing 0.5″. Air flow is 500 lfpm along the Z axis.

The majority of MECL 10H, MECL 10K, and MECL III users employ some form of air–flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipations. Table 13 provides gradient data at power levels of 200 mW, 250 mW, 300 mW, and 400 mW with an air flow rate of 500 lfpm. These figures show the proportionate increase in the junction temperature of each dual–in–line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

OPTIMIZING THE LONG TERM RELIABILITY OF PLASTIC PACKAGES

Todays plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However when the ultimate in system reliability is required, thermal management must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperatures are consistent with system reliability goals.

Predicting Bond Failure Time:

Based on the results of almost ten (10) years of +125°C operating life testing, a special arrhenius equation has been developed to show the relationship between junction temperature and reliability.

$$(1)\ T = (6.376 \times 10^{-9})\, e \left[\frac{11554.267}{273.15 + T_J} \right]$$

Where: T = Time in hours to 0.1% bond failure (1 failure per 1,000 bonds).

T_J = Device junction temperature, °C.

And:

$$(2)\ T_J = T_A + P_D\theta_{JA} = T_A + \Delta T_J$$

Where: T_J = Device junction temperature, °C.

T_A = Ambient temperature, °C.

P_D = Device power dissipation in watts.

θ_{JA} = Device thermal resistance, junction to air, °C/Watt.

ΔT_J = Increase in junction temperature due to on–chip power dissipation.

Table 14 shows the relationship between junction temperature, and continuous operating time to 0.1% bond failure, (1 failure per 1,000 bonds).

Table 14. Device Junction Temperature vs. Time to 0.1% Bond Failures

Junction Temp °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Table 14 is graphically illustrated in Figure 24 which shows that the reliability for plastic and ceramic devices are the same until elevated junction temperatures induces intermetallic failures in plastic devices. Early and mid–life failure rates of plastic devices are not effected by this intermetallic mechanism.

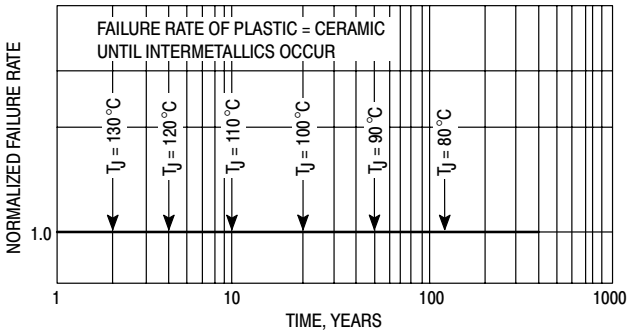


Figure 24. Failure Rate vs. Time Junction Temperature

MECL Junction Temperatures:

Power levels have been calculated for a number of MECL 10K and MECL 10H devices in 20 pin plastic leaded chip carriers and translated to the resulting increase of junction temperature (ΔT_J) for still air and moving air at 500 LFPM using equation 2 and are shown in Table 15.

Table 15. Increase in Junction Temperature Due to I/C Power Dissipation. 20 Pin Plastic Leaded Chip Carrier.

MECL 10K Device Type	ΔT_J, °C Still Air	ΔT_J, °C 500 LFPM Air	MECL 10H Device Type	ΔT_J, °C Still Air	ΔT_J, °C 500 LFPM Air
MC10101	21.8	14.1	MC10H016	48.0	30.0
MC10102	17.6	11.4	MC10H100	16.6	10.8
MC10103	17.6	11.4	MC10H101	22.1	14.5
MC10104	20.8	13.4	MC10H102	18.0	11.8
MC10105	17.2	11.2	MC10H103	18.0	11.8
MC10106	13.0	8.4	MC10H104	21.0	13.5
MC10107	19.8	12.8	MC10H105	17.8	11.7
MC10109	11.7	7.7	MC10H106	13.2	8.7
MC10110	24.7	16.1	MC10H107	20.0	12.9
MC10111	24.7	16.1	MC10H109	11.9	7.8
MC10113	22.2	14.3	MC10H113	22.8	14.8
MC10114	22.6	14.6	MC10H115	16.7	10.9
MC10115	16.7	10.9	MC10H116	17.8	11.7
MC10116	17.2	11.1	MC10H117	16.7	11.0
MC10117	16.2	10.5	MC10H121	13.9	9.1
MC10121	13.5	8.5	MC10H123	23.1	15.0
MC10123	37.6	24.0	MC10H124	44.2	28.4
MC10124	42.9	27.3	MC10H125	–	–
MC10125	–	–	MC10H130	28.2	18.2
MC10131	26.9	17.1	MC10H135	33.2	21.4
MC10133	34.4	21.9	MC10H136	61.7	38.5
MC10134	27.0	17.2	MC10H141	44.3	28.0
MC10135	31.9	20.3	MC10H158	25.3	16.4
MC10136	52.3	32.6	MC10H159	27.3	17.7
MC10138	37.0	23.2	MC10H160	32.1	20.5
MC10141	42.7	26.7	MC10H161	41.5	26.7
MC10153	34.4	21.9	MC10H162	41.5	26.7
MC10158	23.9	15.2	MC10H164	31.9	20.6
MC10159	25.8	16.4	MC10H165	56.3	35.8
MC10160	32.0	20.4	MC10H166	44.4	28.3
MC10161	40.7	26.0	MC10H171	41.9	26.9
MC10162	40.7	26.0	MC10H172	41.9	26.9
MC10164	31.3	20.1	MC10H173	32.6	21.1
MC10165	53.7	33.6	MC10H174	32.5	21.0
MC10166	43.5	27.6	MC10H175	45.9	29.6
MC10168	34.4	21.9	MC10H176	50.9	32.3
MC10170	29.9	18.9	MC10H179	35.0	22.6
MC10171	41.1	26.2	MC10H180	42.4	27.2
MC10172	41.1	26.2	MC10H181 (Note 15)	64.4	38.6
MC10173	30.5	19.3	MC10H186	50.2	31.8
MC10174	31.9	20.5	MC10H188	25.8	16.7
MC10175	43.7	27.6	MC10H189	25.8	16.7
MC10176	49.6	31.3	MC10H209	18.9	12.5
MC10178	38.1	23.9	MC10H210	25.0	16.4
MC10186	49.6	31.1	MC10H211	25.0	16.4
MC10188	25.4	16.4	MC10H330 (Note 15)	65.8	36.1
MC10189	24.6	15.9	MC10H332	52.2	33.5
MC10192	67.0	43.0	MC10H334	77.8	49.3
MC10195	46.7	29.9	MC10H350	–	–
MC10197	27.7	17.7	MC10H351	27.2	18.1
MC10198	21.2	13.4	MC10H352	27.2	18.1
MC10210	24.5	16.0	MC10H424	37.7	24.3
MC10211	24.6	16.0			
MC10212	24.3	15.8			
MC10216	24.1	15.6			
MC10231	30.6	19.5			

12. All ECL outputs are loaded with a 50 Ω resistor and assumed operating at 50% duty cycle.
13. ΔT_J for ECL to TTL translators are excluded since the supply current to the TTL section is dependent on frequency, duty cycle and loading.
14. Thermal Resistance (θ_{JA}) measured with PLCC packages solder attached to traces on 2.24″ x 2.24″ x 0.062″ FR4 type glass epoxy board with 1 oz./sq. ft. copper (solder–coated) mounted to tester with 3 leads of 24 gauge copper wire.
15. 28 lead PLCC.

Case Example:

After the desired system failure rate has been established for failure mechanisms other than intermetallics, each plastic device in the system should be evaluated for maximum junction temperature using Table 15. Knowing the maximum junction temperature refer to Table 14 or Equation 1 to determine the continuous operating time required to 0.1% bond failures due to intermetallic formation. At this time, system reliability departs from the desired value as indicated in Figure 24.

To illustrate, assume that system ambient air temperature is 55°C (an accepted industry standard for evaluating system failure rates). Reference is made to Table 15 to determine the maximum junction temperature for each device for still air and transverse air flow of 500 LFPM.

Adding the 55°C ambient to the highest, ΔT_J listed, 77.8°C (for the MC10H334 with no air flow), gives a maximum junction temperature of 132.8°C. Reference to Table 14 indicates a departure from the desired failure rate after about 2 years of constant exposure to this junction temperature. If 500 LFPM of air flow is utilized, maximum junction temperature for this device is reduced to 104.3°C for which Table 14 indicates an increased failure rate in about 15 years.

Air flow is one method of thermal management which should be considered for system longevity. Other commonly used methods include heat sinks for higher powered devices, refrigerated air flow and lower density board stuffing.

The material presented here emphasizes the need to consider thermal management as an integral part of system design and also the tools to determine if the management methods being considered are adequate to produce the desired system reliability.

THERMAL EFFECTS ON NOISE MARGIN

The data sheet dc specifications for standard MECL 10K and MECL III devices are given for an operating temperature range from –30°C to +85°C (0° to +75°C for MECL 10H and memories). These values are based on having an airflow of 500 lfpm over socket or P/C board mounted packages with no special heatsinking (i.e., dual–in–line package mounted on lead seating plane with no contact between bottom of package and socket or P/C board and flat package mounted with bottom in direct contact with non–metalized area of P/C board).

The designer may want to use MECL devices under conditions other than those given above. The majority of the low–power device types may be used without air and with higher $\overline{\theta}_{JA}$. However, the designer must bear in mind that junction temperatures will be higher for higher $\overline{\theta}_{JA}$, even though the ambient temperature is the same. Higher junction temperatures will cause logic levels to shift.

As an example, a 300 mW 16 lead dual–in–line ceramic device operated at $\overline{\theta}_{JA}$ = 100°C/W (in still air) shows a HIGH logic level shift of about 21 mV above the HIGH logic level when operated with 500 lfpm air flow and a $\overline{\theta}_{JA}$ = 50°C/W. (Level shift = $\Delta T_J \times 1.4$ mV/°C).

If logic levels of individual devices shift by different amounts (depending on P_D and θ_{JA}), noise margins are somewhat reduced. Therefore, the system designer must lay out his system bearing in mind that the mounting procedures to be used should minimize thermal effects on noise margin.

The following sections on package mounting and heatsinking are intended to provide the designer with sufficient information to insure good noise margins and high reliability in MECL system use.

MOUNTING AND HEATSINK SUGGESTIONS

With large high–speed logic systems, the use of multilayer printed circuit boards is recommended to provide both a better ground plane and a good thermal path for heat dissipation. Also, a multilayer board allows the use of microstrip line techniques to provide transmission line interconnections.

Two–sided printed circuit boards may be used where board dimensions and package count are small. If possible, the V_{CC} ground plane should face the bottom of the package to form the thermal conduction plane. If signal lines must be placed on both sides of the board, the V_{EE} plane may be used as the thermal plane, and at the same time may be used as a pseudo ground plane. The pseudo ground plane becomes the ac ground reference under the signal lines placed on the same side as the V_{CC} ground plane (now on the opposite side of the board from the packages), thus maintaining a microstrip signal line environment.

Two–ounce copper P/C board is recommended for thermal conduction and mechanical strength. Also, mounting holes for low power devices may be countersunk to allow the package bottom to contact the heat plane. This technique used along with thermal paste will provide good thermal conduction.

Printed channeling is a useful technique for conduction of heat away from the packages when the devices are soldered into a printed circuit board. As illustrated in Figure 25, this heat dissipation method could also serve as V_{EE} voltage distribution or as a ground bus. The channels should terminate into channel strips at each side or the rear of a plug–in type printed circuit board. The heat can then be removed from the circuit board, or board slide rack, by means of wipers that come into thermal contact with the edge channels.

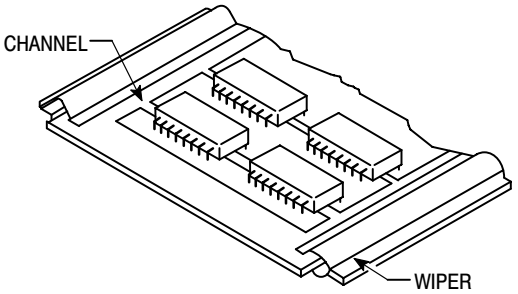


Figure 25. Channel/Wiper Heatsinking on Double Layer Board

For operating some of the higher power device types* in 16 lead dual–in–line packages in still air, requiring $\overline{\theta}_{JA}$ <100°C/W, a suitable heatsink is the IERC LIC–214A2WCB shown in Figure 26. This sink reduces the still air $\overline{\theta}_{JA}$ to around 55°C/W. By mounting this heatsink directly on a copper ground plane (using silicone paste) and passing 500 lfpm air over the packages, $\overline{\theta}_{JA}$ is reduced to approximately 35°C/W, permitting use at higher ambient temperatures than +85°C (+75°C for MECL 10H memories) or in lowering T_J for improved reliability.

*10136 and 10H136 Max P_D > 800 mW.

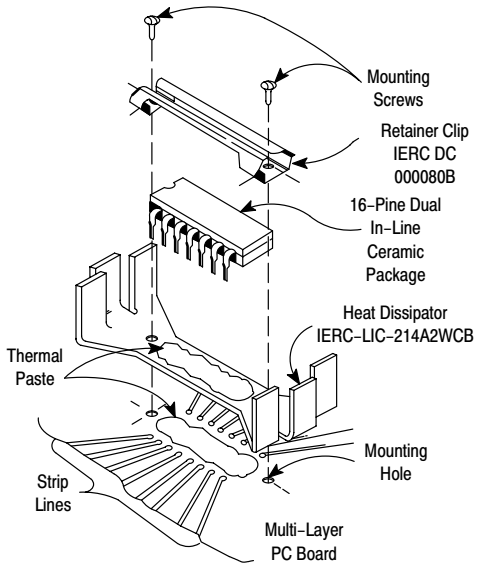


Figure 26. MECL High–Power Dual–In–Line Package Mounting Method

It should be noted that the use of a heatsink on the top surface of the dual–in–line package is not very effective in lowering the $\overline{\theta}_{JA}$. This is due to the location of the die near the bottom surface of the package. Also, very little (< 10%) of the internal heat is withdrawn through the package leads due to the isolation from the ceramic by the solder glass seals and the limited heat conduction from the die through 1.0 to 1.5 mil aluminum bonding wires.

INTERFACING MECL TO SLOWER LOGIC TYPES

MECL circuits are interfaceable with most other logic forms. For MECL/TTL/DTL interfaces, when MECL is operated at the recommended –5.2 volts and TTL/DTL at +5.0 V supply, currently available translator circuits, such as the MC10124 and MC10125, may be used.

For systems where a dual supply (–5.2 V and +5.0 V) is not practical, the MC10H350 includes four single supply MECL to TTL translators, or a discrete component translator can be designed. For details, see MECL System Design Handbook (HB205/D). Such circuits can easily be made fast enough for any available TTL.

MECL also interfaces readily with MOS. With CMOS operating at +5.0 V, any of the MECL to TTL translators works very well.

Specific circuitry for use in interfacing MECL families to other logic types is given in detail in the MECL System Design Handbook.

Complex MECL 10K devices are presently available for interfacing MECL with MOS logic, MOS memories, TTL three–state circuits, and IBM bus logic levels. See Application Note AN720/D for additional interfacing information.

CIRCUIT INTERCONNECTIONS

Though not necessarily essential, the use of multilayer printed circuit boards offers a number of advantages in the development of high–speed logic cards. Not only do multilayer boards achieve a much higher package density, interconnecting leads are kept shorter, thus minimizing propagation delay between packages. This is particularly beneficial with MECL III which has relatively fast (1.0 ns) rise and fall times. Moreover, the unbroken ground planes made possible with multilayer boards permit much more precise control of transmission line impedances when these are used for interconnecting purposes. Thus multilayer boards are recommended for MECL III layouts and are justified when operating MECL 10H and MECL 10K at top circuit speed, when high–density package is a requirement, or when transmission line interconnects are used.

Point–to–point back–plane wiring without matched line terminations may be employed for MECL interconnections if line runs are kept short. At MECL 10K speeds, this applies to line runs up to 6 inches, for MECL 10H and MECL III up to 1 inch (Maximum open wire lengths for less than 100 mV undershoot). But, because of the open–emitter outputs of MECL 10H, MECL 10K and MECL III circuits, pull–down resistors are always required. Several ways of connecting such pull–down resistors are shown in Figures 27, 28, and 29.

Resistor values for the connection in Figure 27 may range from 270 ohms to kΩ depending on power and load requirements. (See MECL System Design Handbook.) Power may be saved by connecting pull–down resistors in the range of 50 ohms to 150 ohms, to –2.0 Vdc, as shown in Figure 28. Use of a series damping resistor, Figure 29, will extend permissible lengths of unmatched–impedance interconnections, with some loss of edge speed.

With proper choice of the series damping resistor, line lengths can be extended to any length,** while limiting overshoot and undershoot to a predetermined amount. Damping resistors usually range in value from 10 ohms to 100 ohms, depending on the line length, fanout, and line impedance, the open emitter–follower outputs of MECL 10H, MECL III and MECL 10K give the system designer all possible line driving options.

One major advantage of MECL over saturated logic is its capability for driving matched–impedance transmission lines. Use of transmission lines retains signal integrity over long distances. The MECL 10H and MECL 10K emitter–follower output transistors will drive a 50–ohm transmission line terminated to –2.0 Vdc. This is the equivalent current load of 22 mA in the HIGH logic state and 6.0 mA in the LOW state.

Parallel termination of transmission lines can be done in two ways. One, as shown in Figure 30, uses a single resistor whose value is equal to the impedance (Z_o) of the line. A terminating voltage (V_{TT}) of –2.0 Vdc must be supplied to the terminating resistor.

Another method of parallel termination uses a pair of resistors, R1 and R2. Figure 31 illustrates this method. The following two equations are used to calculate the values of R1 and R2:

$$R1 = 1.6\ Z_o$$
$$R2 = 2.6\ Z_o$$

Another popular approach is the series–terminated transmission line (see Figures 30 and 31). This differs from parallel termination in that only one–half the logic swing is propagated through the lines. The logic swing doubles at the end of the transmission line due to reflection on an open line, again establishing a full logic swing.

Pull–Down Resistor Techniques

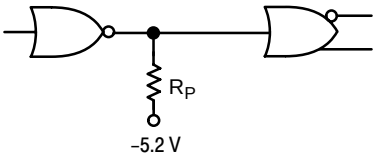


Figure 27.

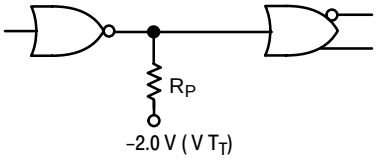


Figure 28.

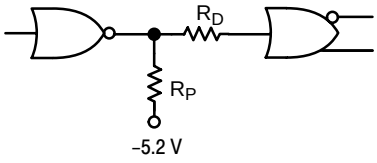


Figure 29.

To maintain clean wave fronts, the input impedance of the driven gate must be much greater than the characteristic impedance of the transmission line. This condition is satisfied by MECL circuits which have high impedance inputs. Using the appropriate terminating resistor (R_S) at point A (Figure 32), the reflections in the transmission line will be terminated.

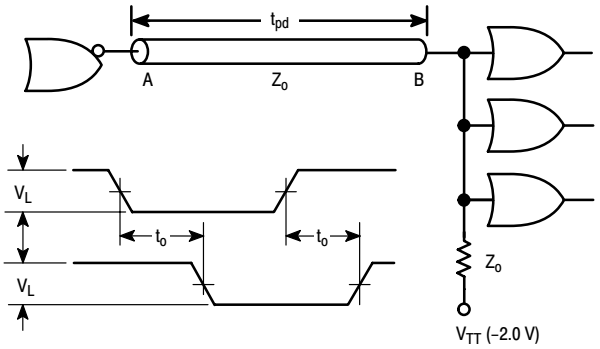


Figure 30. Parallel Terminated Line

** Limited only by line attenuation and band–width characteristics.

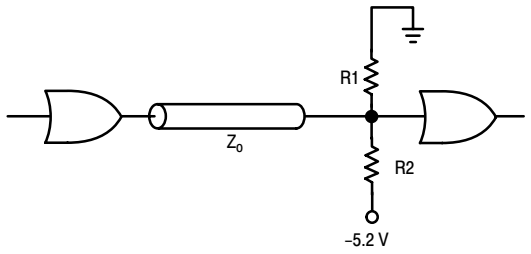


Figure 31. Parallel Termination – Thevenin Equivalent

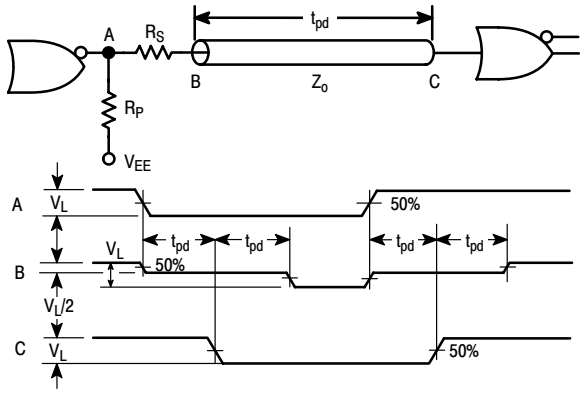


Figure 32. Series Terminated Line

The advantages of series termination include ease of driving multiple series–terminated lines, low power consumption, and low cross talk between adjacent lines. The disadvantage of this system is that loads may not be distributed along the transmission line due to the one–half logic swing present at intermediate points.

For board–to–board interconnections, coaxial cable may be used for signal conductors. The termination techniques just discussed also apply when using coax. Coaxial cable has the advantages of good noise immunity and low attenuation at high frequencies.

Twisted pair lines are one of the most popular methods of interconnecting cards or panels. The complementary outputs of any MECL function may be connected to one end of the twisted pair line, and any MECL differential line receiver to the other as shown in the example, Figure 33. R_T is used to terminate the twisted pair line. The 1 to 1.5 V common–mode noise rejection of the line receiver ignores common–mode cross talk, permitting multiple twisted pair lines to be tied into cables. MECL signals may be sent very long distances (> 1000 feet) on twisted pair, although line attenuation will limit bandwidth, degrading edge speeds when long line runs are made.

If timing is critical, parallel signals paths (shown in Figure 34) should be used when fanout to several cards is required. This will eliminate distortion caused by long stub lengths off a signal path.

Wire–wrapped connections can be used with MECL 10K. For MECL III and MECL 10H, the fast edge speeds (1.0 ns) create a mismatch at the wire–wrap connections which can cause reflections, thus reducing noise immunity. The mismatch occurs also with MECL 10K, but the distance between the wire–wrap connections and the end of the line is generally short enough so the reflections cause no problem.

Series damping resistors may be used with wire–wrapped lines to extend permissible backplane wiring lengths. Twisted pair lines may be used for even longer distances across large wire–wrapped cards. The twisted pair gives a more defined characteristic impedance (than a single wire), and can be connected either single–ended, or differentially using a line receiver.

The recommended wire–wrapped circuit cards have a ground plane on one side and a voltage plane on the other side to insure a good ground and a stable voltage source for the circuits. In addition, the ground plane near the wire–wrapped lines lowers the impedance of those lines and facilitates terminating the line. Finally, the ground plane serves to minimize cross talk between parallel paths in the signal lines. Point–to–point wire routing is recommended because cross talk will be minimized and line lengths will be shortest. Commercial wire–wrap boards designed for MECL 10K are available from several vendors.

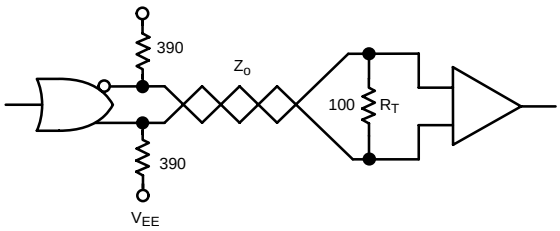
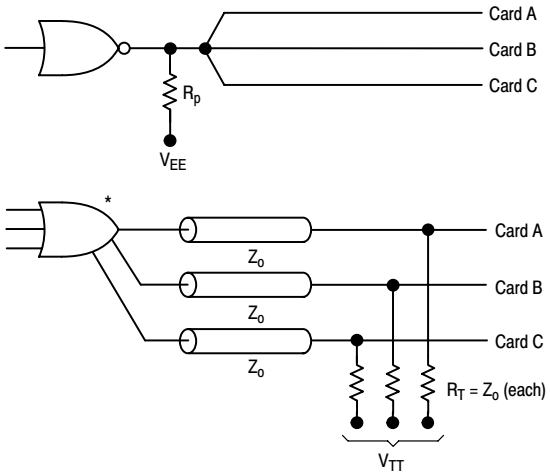


Figure 33. Twisted Pair Line Driver/Receiver



*Multiple output gate eg MC10110

Figure 34. Parallel Fanout Techniques

Microstrip and Stripline

Microstrip and stripline techniques are used with printed circuit boards to form transmission lines. Microstrip consists of a constant–width conductor on one side of a circuit board, with a ground plane on the other side (shown in Figure 35). The characteristic impedance is determined by the width and thickness of the conductor, the thickness of the circuit board, and the dielectric constant of the circuit board material.

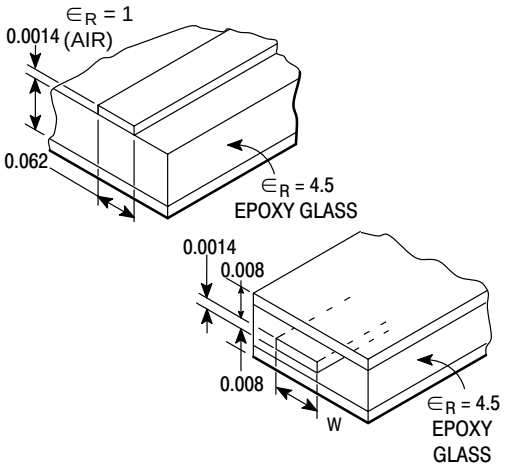


Figure 35. PC Interconnection Lines for use with MECL

Stripline is used with multilayer circuit boards as shown in Figure 35. Stripline consists of a constant–width conductor between two ground planes.

Refer to MECL System Design Handbook for a full discussion of the properties and use of these.

CLOCK DISTRIBUTION

Clock distribution can be a system problem. At MECL 10K speeds, either coaxial cable or twisted pair line (using the MC10101 and MC10115) can be used to distribute clock signals throughout a system. Clock line lengths should be controlled and matched when timing could be critical. Once the clocking signals arrive on card, a tree distribution should be used for large–fanouts at high frequency. An example of the application of the technique is shown in Figure 36.

Because of the very high clock rates encountered in MECL III systems, rules for clocking are more rigorous than in slower systems.

The following guidelines should be followed for best results:

On–Card Synchronous Clock Distribution via Transmission Line

1. Use the NOR output in developing clock chains or trees. Do not mix OR and NOR outputs in the chain.
2. Use balanced fanouts on the clock drivers.
3. Overshoot can be reduced by using two parallel drive lines in place of one drive line with twice the lumped load.

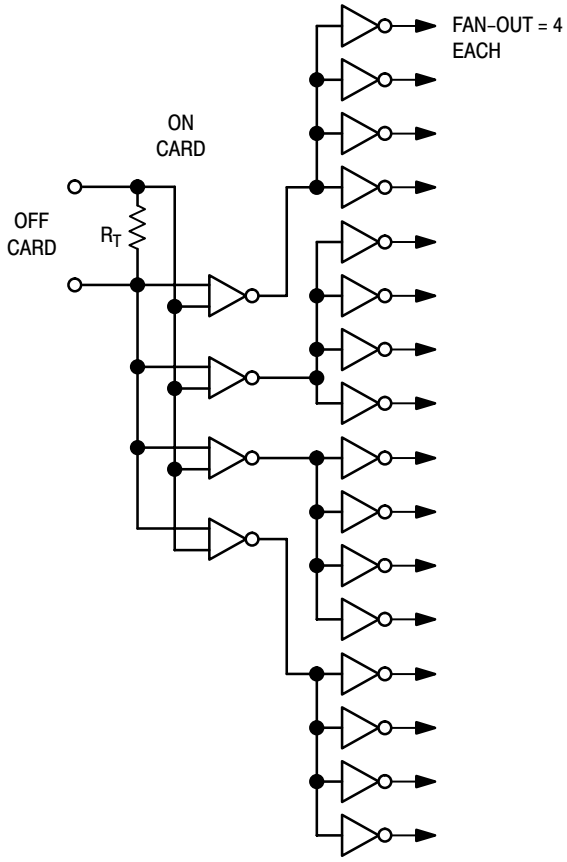


Figure 36. 64 Fanout Clock Distribution (Proper Termination Required)

4. To minimize clock skewing problems on synchronous sections of the system, line delays should be matched to within 1.0 ns.
5. Parallel drive gates should be used when clocking repetition rates are high, or when high capacitance loads occur. The bandwidth of a MECL III gate may be extended by paralleling both halves of a dual gate. Approximately 40 or 50 MHz bandwidth can be gained by paralleling two or three clock driver gates.
6. Fanout limits should be applied to clock distribution drivers. Four to six loads should be the maximum load per driver for best high speed performance. Avoid large lumped loads at the end of lines greater than 3 inches. A lumped load, if used, should be four or fewer loads.
7. For wire–OR (emitter dotting), two–way lines (busses) are recommended. To produce such lines, both ends of a transmission line are terminated with 100–ohm impedance. This method should be used when wire–OR connections exceed 1 inch apart on a drive line.

Off–Card Clock Distribution

1. The OR/NOR outputs of an MC1660 may be used to drive into twisted pair lines or into flat, fixed–impedance ribbon cable. At the far end of the twisted pair on MC1692 differential line receiver is used. The line should be terminated as shown in Figure 33. This method not only provides high speed, board–to–board clock distribution, but also provides system noise margin advantages. Since the line receiver operates independently of the V_{BB} reference voltage (differential inputs) the noise margin from board to board is also independent of temperature differentials.

LOGIC SHORTCUTS

MECL circuitry offers several logic design conveniences. Among these are:

1. **Wire–OR** (can be produced by wiring MECL output emitters together outside packages).
2. **Complementary Logic Outputs** (both OR and NOR are brought out to package pins in most cases).

An example of the use of these two features to reduce gate and package count is shown in Figure 37.

The connection shown saves several gate circuits over performing the same functions with non–ECL type logic. Also, the logic functions in Figure 37 are all accomplished with one gate propagation delay time for best system speed. Wire–ORing permits direct connections of MECL circuits to busses. (MECL System Design Handbook and Application Note AN726/D).

Propagation delay is increased approximately 50 ps per wire–OR connection. In general, wire–OR should be limited to 6 MECL outputs to maintain a proper LOW logic level. The MC10123 is an exception to this rule because it has a special V_{OL} level that allows very high fanout on a bus or wire–OR line. The use of a single output pull–down resistor is recommended per wire–OR, to economize on power dissipation. However, two pull–down resistors per wired–OR can improve fall times and be used for double termination of busses.

Wire–OR should be done between gates in a package or nearby packages to avoid spikes due to line propagation delay. This does not apply to bus lines which activate only one driver at a time.

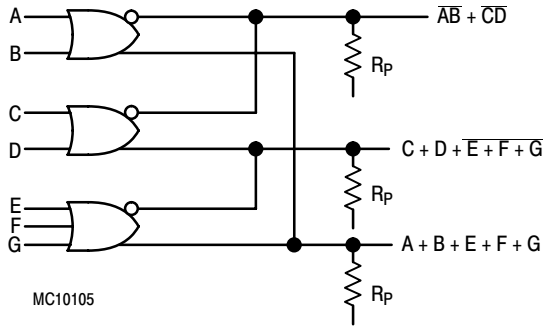


Figure 37. Use of Wire–OR and Complementary Outputs

Table 16. System Considerations – A Summary of Recommendations

	MECL 10H	MECL 10K
Power Supply Regulation	±5% (Note 16)	10% (Note 17)
On–Card Temperature Gradient	20°C	Less Than 25°C
Maximum Non–Transmission Line Length (No Damping Resistor)	1″	8″
Unused Inputs	Leave Open (Note 18)	Leave Open (Note 18)
PC Board	Multilayer	Standard 2–Sided or Multilayer
Cooling Requirements	500 lfpm Air	500 lfpm Air
Bus Connection Capability	Yes (Wire–OR)	Yes (Wire–OR)
Maximum Twisted Pair Length (Differential Drive)	Limited by Cable Response Only, Usually >1000′	Limited by Cable Response Only, Usually >1000′
The Ground Plane to Occupy Percent Area of Card	>75%	>50%
Wire Wrap may be used	Not Recommended	Yes
Compatible with MECL 10,000	Yes	–

16. All DC and AC parameters guaranteed for V_{EE} = –5.2 V ± 5%.
17. At the devices (functional only).
18. Except special functions without input pull–down resistors.

Notes

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