NEC
μPD3301-1
μPD3301-2
PRELIMINARY

PROGRAMMABLE CRT CONTROLLER

DESCRIPTION

The μPD3301 is an LSI chip designed for use in CRT controllers. It contains a synchronous signal generator, row buffer, and attribute memory. This CRT controller is capable of handling not only black and white CRT, but also color CRT. The μPD3301 provides control signals which simplify the design of the external circuitry needed in the systems. Thus, this device is a versatile controller that relieves the main CPU (and users) of many of the control burdens associated with implementing a CRT interface.

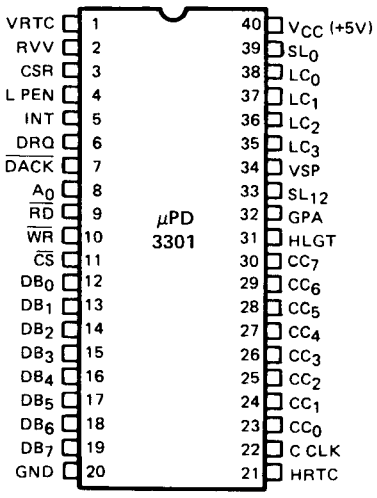
There are 8 separate commands which the μPD3301 will execute. Some of these commands require multiple bytes to fully specify the operation which the processor wishes the CRT controller to perform. The following commands are available:

- RESET
- SET INTERRUPT MASK
- RESET INTERRUPT
- STOP DISPLAY
- READ LIGHT PEN
- RESET COUNTERS
- START DISPLAY
- LOAD CURSOR POSITION

FEATURES

- Programmable Screen and Character Format Capabilities;
  - Characters per Row (up to 80 characters/row)
  - Lines per Character (up to 32 lines/character)
  - Rows per Frame (up to 64 rows/frame)
  - Horizontal Retrace Time
  - Vertical Retrace Time
  - Blinking Time
  - DMA Control Mode
  - Cursor Control Mode
- Three Independent Visual Field Attribute Modes such as;
  - Transparent Attribute Color Mode
  - Transparent Attribute Black and White Mode
  - Non-Transparent Attribute Black and White Mode
- 12 Independent Field Attribute Functions such as;
  - Vertical Line
  - Over-Line
  - Reverse Video
  - Secret
  - Blue
  - Red
  - Under-Line
  - High-Light
  - Blinking
  - General Purpose
  - Green
  - General Purpose Color
- Light Pen Detection
- Maximum 256 Different Characters Control Capability
- Fully Bus Compatible with 8080
- 3 MHz Single Clock Input
- Single Power Supply, +5V N-MOS Technology
- Available in 40 pin Plastic and Ceramic Dual-In-Line Packages

PIN CONFIGURATION

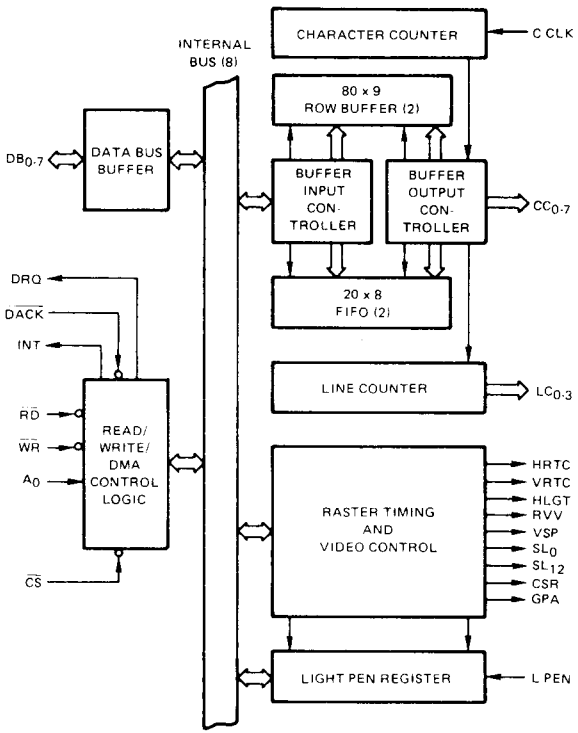


PIN NAMES

VRTC	Vertical Retrace
RVV	Reverse Video
CSR	Cursor
L PEN	Light Pen
INT	Interrupt
DRQ	DMA Request
$\overline{DACK}$	DMA Acknowledge
A_0	Address Bus 0
$\overline{RD}$	Read
$\overline{WR}$	Write
$\overline{CS}$	Chip Select
DB_{0-7}	Data Bus 0 to 7
HRTC	Horizontal Retrace
C CLK	Character Clock
CC_{0-7}	Character Codes 0 to 7
HLGT	High-light
GPA	General Purpose Attribute
SL_{12}	Slit Line 12
VSP	Video Suppression
LC_{0-3}	Line Counter 0 to 3
SL_0	Slit Line 0

9

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Character Counter

Counts the characters in a row, up to the number of the characters defined in Characters/Row.

Row Buffer

Consists of a dual RAM buffer. Each buffer can store up to 80 characters. During a DMA operation, the characters are written into the Row Buffer. One of the buffers is used for display. Each character in the buffer is read with Character Clock (C CLK), and the data appears in CC_{0-7}. At the same time, the data on the next row is written into another buffer by DMA control.

Buffer Input/Output Controller

- Writes the characters into the Row Buffer, up to the number defined by Characters/Row.
- Outputs the data from the Row Buffer to CC_{0-7}.
- Writes the attributes and special control character codes into the FIFO, up to the number defined by Attributes/Row.
- Reads the attribute codes from the FIFO and transfers them to the video circuit.
- In case of Non-Transparent Attribute Mode, it distinguishes an ordinary character code from an attribute code among the character data read from the Row Buffer.

FIFO (First Input, First Output)

Consists of a dual RAM buffer. Each buffer can store up to 20 characters. By DMA operation, attribute codes and special control characters are written into the FIFO. One of the buffers is used for display. Whenever the read flag bit for FIFO is detected, an attribute code is read and transferred to the video circuit. And at the same time, the attribute codes in the next row are written into the rest of the buffers (another buffer) by DMA operation.

FUNCTIONAL DESCRIPTION (CONT.)

Line Counter

Counts the events of Rasters/Line, up to the number indicated by Lines/Character.

Raster Timing and Video Control

- Outputs the HRTC based on the Character Counter during the time indicated by Horizontal Retrace Time.
- Outputs the VRTC based on Row Counter which counts up the contents, row by row, during the time indicated by Vertical Retrace Time.
- Outputs HLGT, RVV, VSP, SL_0, SL_{12}, GPA based on attribute codes transferred from the Buffer Output Controller.
- Outputs the CSR based on the Blinking Time etc. at the position indicated by Cursor Address.

Light Pen Register

Memorizes a row address and column address when the L PEN signal is input. By using READ LIGHT PEN instruction, the CPU can read the contents.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
All Output Voltages . . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −0.5 to +7 Volts
Supply Voltage V_{CC} . . . . . −0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.6 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	DB_{0-7}: I_{OH} = -150 μA, All Others: -80 μA
Low Level Input Leakage	I_{IL}			-10	μA	V_{IN} = 0V
High Level Input Leakage	I_{IH}			+10	μA	V_{IN} = V_{CC}
Low Level Output Leakage	I_{OL}			-10	μA	V_{OUT} = 0V
High Level Output Leakage	I_{OH}			+10	μA	V_{OUT} = V_{CC}
Power Supply Current	I_{CC}		90		mA	

CAPACITANCE

T_a = 25°C; V_{CC} = 0V

PARAMETER	SYMBOL	LIMITS		UNIT	TEST CONDITIONS
		MIN	MAX		
Input Capacitance	C_{IN}		10	pF	fc = 1 MHz, All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}		20	pF	

9

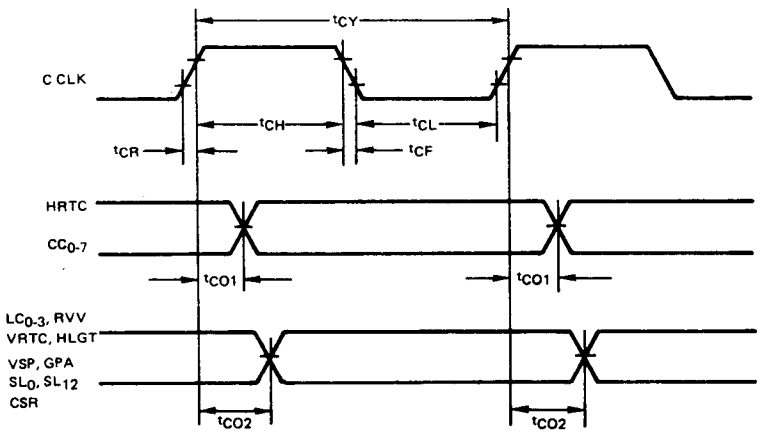
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER		SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Cycle Time	μPD3301-1	t_{CY}	0.5	10	μs	
	μPD3301-2	t_{CY}	0.38	10	μs	
Clock High Level		t_{CH}	150		ns	
Clock Low Level		t_{CL}	150	1000	ns	
Clock Rise Time		t_{CR}	5	30	ns	
Clock Fall Time		t_{CL}	5	30	ns	
Output Delay from C CLK ↑		t_{CO1}	0	150	ns	1TTL + 15 pF: HRTC, CC_{0-7}
Output Delay from C CLK ↑	μPD3301-1	t_{CO2}		400	ns	1TTL + 15 pF: Except HRTC, CC_{0-7}
	μPD3301-2	t_{CO2}		300	ns	
Command Cycle Time		t_E	$2t_{CY}$ + 200		ns	$t_{CY} \geq 400$ μs
		t_E	1		μs	$t_{CY} < 400$ μs
A_0, $\overline{CS}$ Set Up Time to $\overline{WR}$		t_{AW}	0		ns	
A_0, $\overline{CS}$ Hold Time to $\overline{WR}$		t_{WA}	0		ns	
$\overline{WR}$ Pulse Width		t_{WW}	200		ns	
Data Set Up Time to $\overline{WR}$		t_{DW}	150		ns	
Data Hold Time to $\overline{WR}$		t_{WD}	30		ns	
$\overline{DACK}$ ↓ Set Up Time to $\overline{WR}$		t_{KW}	0		ns	
$\overline{DACK}$ ↑ Hold Time to $\overline{WR}$		t_{WK}	0		ns	
DRQ Delay from $\overline{DACK}$ ↓		t_{KQ}	0	250	ns	1TTL + 50 pF
INT Delay from $\overline{WR}$ ↑		t_{WI}	t_{CY} + 20	$2t_{CY}$ + 300	ns	1TTL + 50 pF
INT Delay from C CLK ↑		t_{CI}		300	ns	1TTL + 50 pf
A_0, $\overline{CS}$ Set Up Time to $\overline{RD}$		t_{AR}	0		ns	
A_0, $\overline{CS}$ Hold Time to $\overline{RD}$		t_{RA}	0		ns	
$\overline{RD}$ Pulse Width		t_{RR}	300		ns	
Data Access Time from $\overline{RD}$ ↓		t_{RD}	0	250	ns	C_L = 100 pF
Data Float Delay from $\overline{RD}$ ↑		t_{DR}		150	ns	C_L = 100 pF
			20		ns	C_L = 15 pF

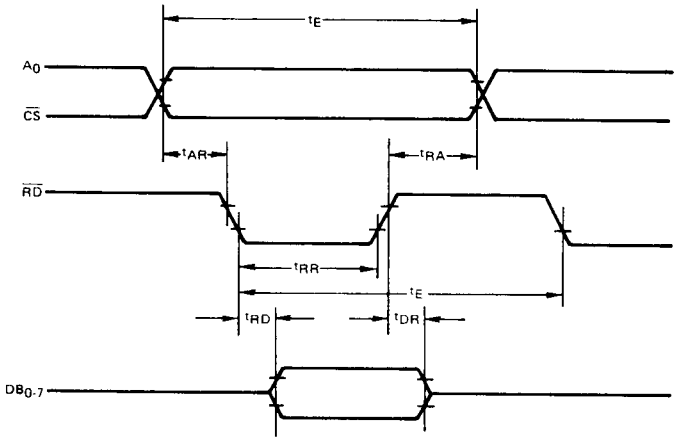
TIMING WAVEFORMS

CLOCK AND OUTPUT DELAY

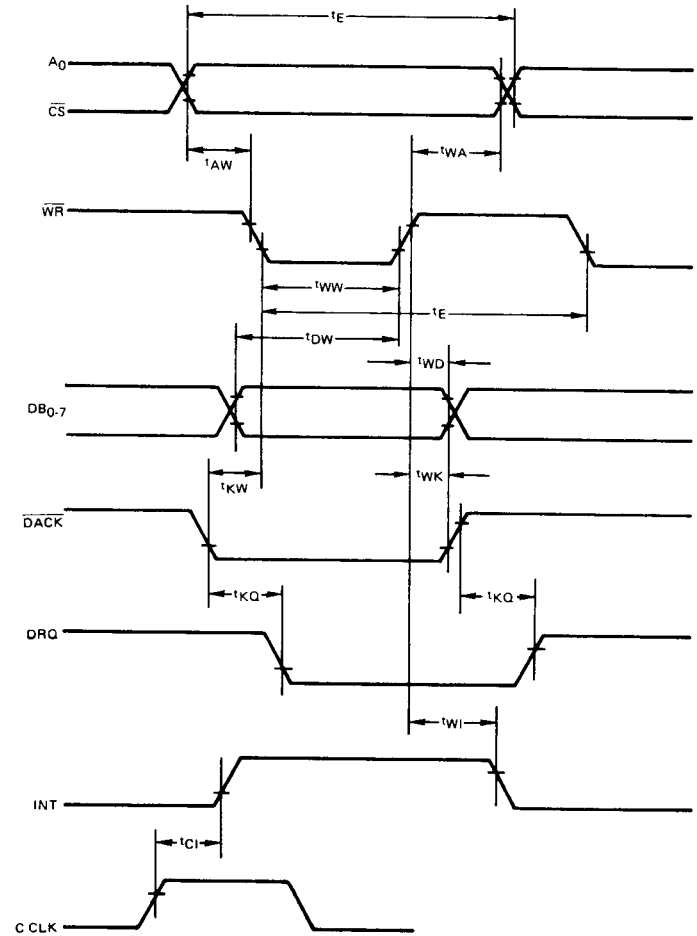


TIMING WAVEFORMS (CONT.)

READ OPERATION



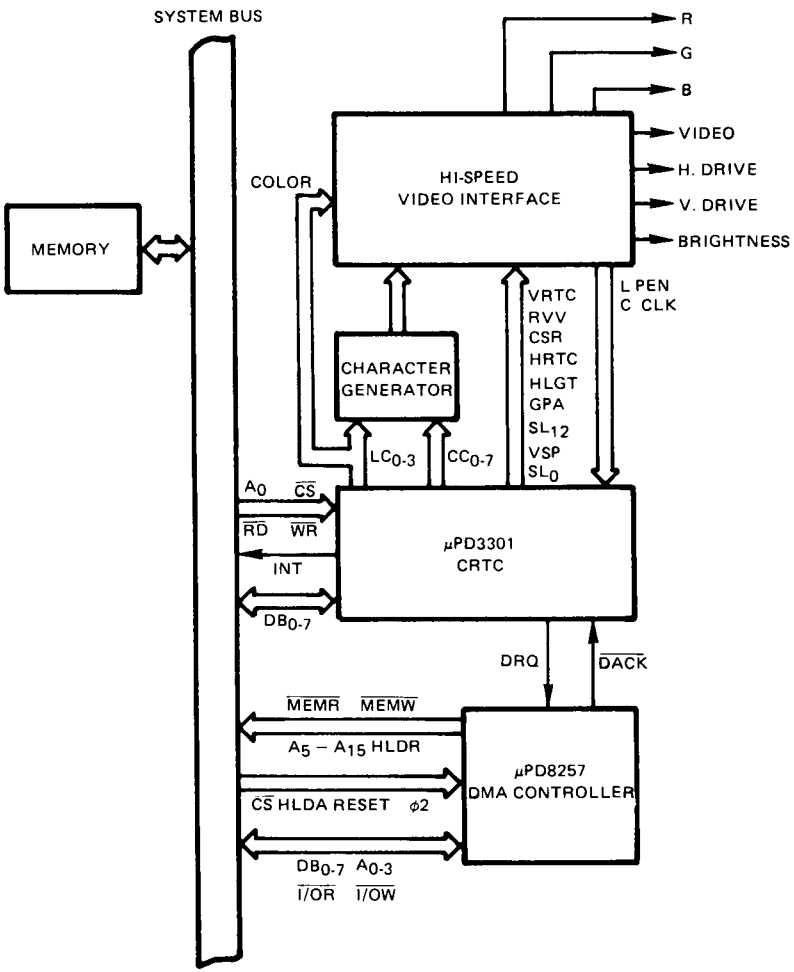
DMA, INTERRUPT AND WRITE OPERATION



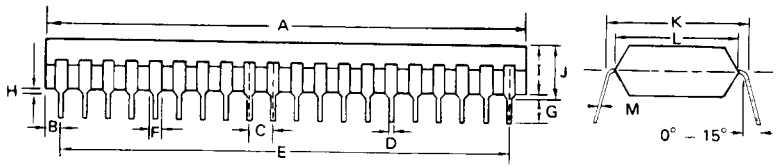
9

SYSTEM CONFIGURATION

The data is transferred from the external memory which contains the information about characters and attributes to the Row Buffer under the control of μPD8257 DMA Controller. The data read from the Row Buffer are Video Control Outputs and ROM Address Signal Outputs toward External Character Generator. The μPD3301 also outputs horizontal and vertical retrace signals.



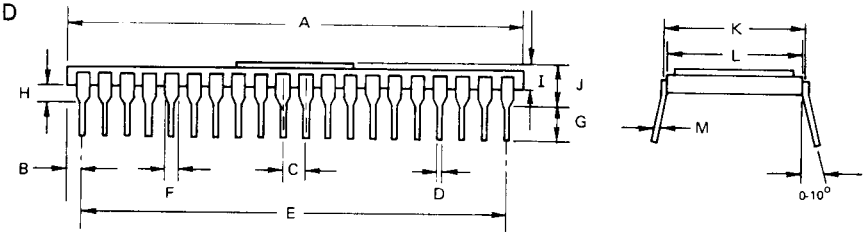
PACKAGE OUTLINES
μPD3301C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.028 MAX.
B	1.62 MAX.	0.064 MAX.
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.2 MIN.	0.047 MIN.
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.019 MIN.
I	5.22 MAX.	0.206 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24 TYP.	0.600 TYP.
L	13.2 TYP.	0.520 TYP.
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

μPD3301D



(CERAMIC)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX.	2.03 MAX.
B	1.62 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.0019

9