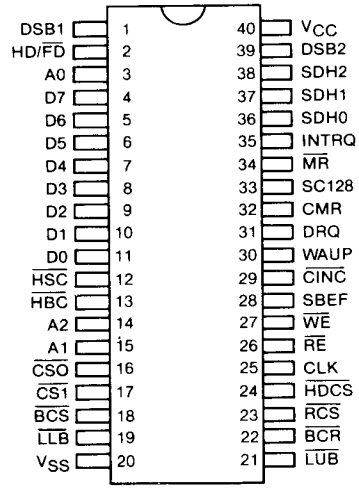
WD1014 Error Detection/Support Logic Device

FEATURES

- 32-BIT ECC POLYNOMIAL
- BURST CORRECTION TO 11-BITS
- MULTIPLE ERROR BURST DETECTION
- DATA TRANSFER RATE OF 5-MBITS/SECOND
- PROCESSES CHECK/SYNDROME BITS IN 2-BIT SERIAL FASHION
- SECTOR SIZES = 128, 256, 512, & 1024 BYTE DATA FIELDS
- SUPPORT READ/WRITE SHORT/LONG FEATURES
- ON-CHIP STORAGE OF SYNDROME/CHECK BYTES
- 8-BIT I/O DATA BUS
- SOFTWARE ADDRESSABLE REGISTERS & LATCHES
- ON-CHIP LOGIC FOR EXTERNAL BUFFER CONTROL
- 40 PIN, DUAL-IN-LINE, N-MOS DEVICE
- TTL, MOS COMPATABILITY
- SINGLE SOURCE +5 VDC SUPPLY



PIN DESIGNATION

DESCRIPTION

The WD1014 EDS logic chip provides the WD1002-05 Winchester Floppy Disk Controller (WFC) board with ECC and support logic. The EDS chip is a single chip device specifically designed to add error correction capabilities to a 5.25" and 8" Winchester disk drive. It also contains three 8-bit registers, three counters, and several latches that enhance the capability of the WFC on-board Control Processor (CP) chip WD1015 for control functions in real time operation. The EDS 40-pin device replaces approximately 35 standard TTL packages consisting of shift registers, flip-flops, and logic gates.

The ECC polynomial selected is the same as the one implemented in the WD1100-06 ECC/CRC logic except that the current design is a 2-bit serial implementation of the polynomial for faster operation. The ECC polynomial selected is a computer generated code optimized for sector sizes of 128, 256, 512, and 1024 byte data fields. The four ECC bytes appended by this chip enable corection of a single burst of up to 11 bits. It can also simultaneously detect a single burst of up to 20 bits and a double burst of up to 4 bits. The computer generated code has been selected over a comparable fire code since the fire codes suffer from pattern sensitivity problem.

The WD1014 EDS device is fabricated using N-channel silicone gate technology, and is available in a 40-pin, ceramic, dual-in-line package.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	PIN NAME	FUNCTION
1	DSB1	DRIVE SELECT BIT 1	This output is encoded with DSB2 to select one of three Winchester Drives or one of four floppy drives depending upon the state of HD / FD.
2	HD / $\overline{FD}$	HARD OR $\overline{FLOPPY}$ DISK SELECT	When high, hard disk drives are selected and when low, floppy disk drives are selected.
3	A0	ADDRESS BIT 0	This input along with $\overline{CS0}$ = 1 and $\overline{CS1}$ = 0 is used to address the WD 1014 registers.
4 Thru 11	D7 thru D0	DATA 7 thru DATA 0	8-bit bi-directional data bus. Data is output only when the check / syndrome register or the command register is read.
12	$\overline{HSC}$	$\overline{HOST\ STATUS}$ CONTROL	This output when low, enables the WFC status onto the data lines making them available to the Host processor, if WAUP = 0.
13	$\overline{HBC}$	$\overline{HOST\ BUS\ CONTROL}$	This output when low, enables the Host to communicate to the WFC and set up all task files, if WAUP = 0 and $\overline{HSC}$ = 1.
14 15	A2 A1	ADDRESS BIT 2 ADDRESS BIT 1	These 2 inputs along with $\overline{CS0}$ = 1 and $\overline{CS1}$ = 0 are used to address the WD1014 registers.
16 17	$\overline{CS0}$ $\overline{CS1}$	$\overline{CHIP\ SELECT\ BIT\ 0}$ $\overline{CHIP\ SELECT\ BIT\ 1}$	$\overline{CS0}$ = 1 and $\overline{CS1}$ = 0 selects the WD1014, for other combinations see the chart under task files.
18	$\overline{BCS}$	$\overline{BUFFER\ CHIP\ SELECT}$	This input line indicates that an external device wants to access the buffer. The ECC check / syndrome computation is also enabled at this time.
19	$\overline{LLB}$	$\overline{LOAD\ LOWER\ BYTE}$	The rising edge of this output line is used to load the lower byte of address into the external buffer counter.
20	V_{SS}	GROUND	Ground.
21	$\overline{LUB}$	$\overline{LOAD\ UPPER\ BYTE}$	The rising edge of this output line is used to load the upper byte of address into the external buffer counter.
22	$\overline{BCR}$	$\overline{BUFFER\ COUNTER\ RESET}$	This input indicates that an external device wants to reset the external buffer counters. The internal overflow counters are also cleared.
23	$\overline{RCS}$	$\overline{RAM\ CHIP\ SELECT}$	This output line is used to select external RAM when $\overline{BCS}$ is active low or when the CP or the Host is accessing the RAM. This output is disabled when SBEF = 1.
24	$\overline{HDCS}$	$\overline{HARD\ DISK\ CHIP\ SELECT}$	This output line is used to enable the WD1010 when the Host is accessing its task files except the Error, Status and Command registers.
25	CLK	CLOCK	The rising edge of CLK is used to shift the ECC polynomial and the falling edge is used to count exactly 4 shifts.
26 27	$\overline{RE}$ $\overline{WE}$	$\overline{READ\ ENABLE}$ $\overline{WRITE\ ENABLE}$	Strobes used in conjunction with $\overline{CS0}$ = 1, $\overline{CS1}$ = 0, A2-A0 to access registers.
28	SBEF	SECTOR BUFFER EMPTY OR FULL	Output signal used to indicate the sector buffer has been filled or emptied.
29	$\overline{CINC}$	$\overline{COUNTER\ INCREMENT}$	The rising edge of this output signal increments an external address counter. This output is enabled only if the RAM is being accessed and SBEF = 0.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	PIN NAME	FUNCTION
30	WAUP	WAKEUP	This output signal is made active by the Host issuing a command and filling the sector buffer. It indicates that a command is being executed by the CP on the WFC board. The Host now cannot communicate with the WFC until the command has been completed. $\overline{MR}$ also sets WAUP.
31	DRQ	DATA REQUEST	The data request line is activated whenever the sector buffer contains data to be read by the Host, or is awaiting data to be loaded by the Host. This line is reset whenever the sector buffer has been filled or emptied.
32	CMR	COUNTER MASTER RESET	This output signal resets the external address counters whenever a $\overline{MR}$ or a command has been issued by the Host, or when $\overline{BCS}$ is asserted.
33	SC128	SECTOR COUNT OF 128 BYTES	This input signal is used in conjunction with the SDH register to indicate that the buffer has overflowed.
34	$\overline{MR}$	MASTER RESET	Used to initialize internal logic. All internal buffer overflow counters are reset, the DRQ and INTRQ flip-flops are cleared and BUSY is set.
35	INTRQ	INTERRUPT REQUEST	This output line is activated whenever a command has been completed. It is reset to the inactive state when the status register is read, or a new command is loaded via the DAL lines, or $\overline{MR}$ is asserted.
36 37 38	SDH2 SDH1 SDSH2	DRIVE SELECT, AND HEAD SELECT BITS	The 3 least significant bits of the internal SDH register are available as outputs. The SDH register is updated whenever the Host writes to it.
39	DSB2	DRIVE SELECT BIT 2	This output is encoded with DSB1 to select one of three Winchester Drives or one of four floppy drives depending upon the state of HD/$\overline{FD}$.
40	V_{CC}	POWER SUPPLY	+5V Power Source

TASK FILES

WAKE UP, $\overline{CS1}$, $\overline{CS0}$, A2-A0, $\overline{RE}$ and $\overline{WE}$ are used to select various registers as shown below:

WAKE UP	$\overline{CS1}$	$\overline{CS0}$	A2-A0	EFFECT
X	1	1	X	Idle – Nothing selected.
0	1	0	X	Host to WFC and WD1010 files.
1	1	0	X	CP to WD1010+ RAM access.
1	0	1	X	CP to WD1014.
X	0	0	X	Illegal condition.

A2	A1	A0	WD1014 REGISTERS		WD1010 REGISTERS	
			$\overline{RE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WE}$
0	0	0	0 + CHECK/ SYN bytes*	0 + CHECK bytes*	RAM	RAM
0	0	1		Set ECC	Error Req.**	Write Precomp
0	1	0	SLEEP	0 + LLB[2]	Sector Count	Sector Count
0	1	1	Clear OVF/CNTRS	0 + LUB[2]	Sector Number	Sector Number
1	0	0		Set DRQ	Cylinder Low	Cylinder Low
1	0	1		Set Read Latch	Cylinder High	Cylinder High
1	1	0	Clear Mult Mode	Set Mult Mode	S.D.H.	S.D.H.
1	1	1	0 + Command*	0 + Error Reg.*	Status Reg.**	Command Reg.**

*Data bus contains valid information. Except as indicated in ** the Host and onboard CP(WD1015) can access the registers in the WD1010. The registers in the WD1014 can only be accessed by the WD1015. For the registers not referred to in *, the data bus need not contain valid information.

**The Host does not access these registers in the WD1010 (or WD2797). The content of these registers must be off loaded to an intermediate register for access by the Host.

COMMAND	BITS 7	6	5	4	3	2	1	0
READ	0	0	1	0	I	M	L	0
WRITE	0	0	1	1	0	M	L	0
FORMAT	0	1	0	1	0	0	0	0

COMMAND CODES

For the implementation of parts of the controls, the following command codes are pertinent:

The control logic only decodes bits 7-4 and uses bit 1 (long bit) in its internal logic. The rest of the command codes and bits are not used by the WD1014.

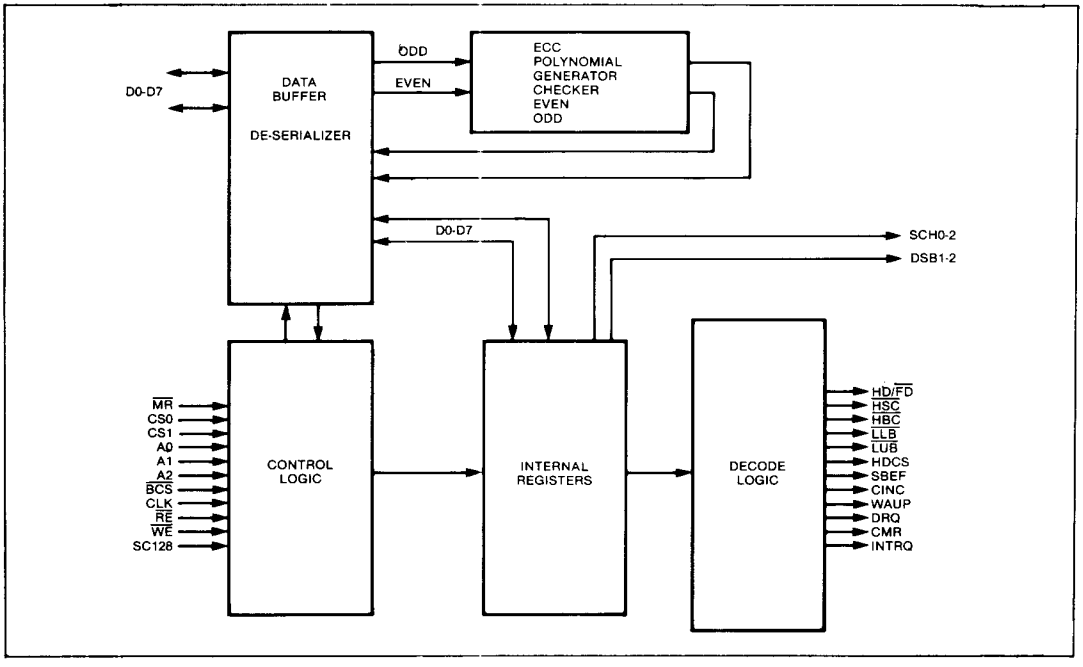
For a complete description of the commands or the task files refer to the WD1002-05 WFC data sheet.

WD1014 ARCHITECTURE

The WD1014 Chip was specifically designed for the WFC board to extend the capabilities of the Control Processor (WD1015) to handle real time functions. As designed, the WD1014 is not a stand alone general purpose device unless, of course, almost all of the protocol described can be used in any new designs.

The WD1014 consists of a 2 bit serial polynomial generator (that produces 4 bytes of check/syndrome) an 8 bit data buffer and deserializer, two 8 bit registers, namely a Command/Error register and a SDH register, and control logic consisting of 3 counters, 6 latches, and a host of combinatorial logic. The addressable registers and latches are accessed as shown in the block diagram below.

Each major functional block will be described essentially independent of one another. Some overlap and references to the WFC board are unavoidable and, in fact, they aid in presenting a clearer picture of the device.



WD1014 BLOCK DIAGRAM

THE ECC POLYNOMIAL GENERATOR

The 4 byte check / syndrome generator consists of two 16 bit shift registers each of which has 8 feedback terms implemented with XOR gates, and control gates for the feedback and data paths.

The leading two bytes of the data field are not recognized by the WD1014. Therefore, in order to maintain compatibility with the devices that do, the polynomial is preset to what would have been calculated if the AIF8 had been read.(B517894A)

ECC computations are made whenever the external sector buffer is being accessed. The data present on the system data bus is accepted by the input data buffer and processed along with the gated data from the last stages of the shift register strings. The direction of shift within the ECC polynomial is from the LS.B. to the M.S.B. After the last byte of data has been accessed from the sector buffer, the internal counter overflow register is set. This in turn sets a feedback inhibit register after the last byte has been processed by the ECC polynomial. At this point, the feedback terms are forced to zero and only the data path to the LS.B. is enabled. This feature is convenient to store the 4 check / syndrome bytes internally so that RLONG and WLONG commands can be supported without the use of an external buffer.

During a write operation, the input data stream is divided by the polynomial and the 32 bit remainder obtained after buffer overflow is used as the 4 check bytes. The 4 check bytes are gated out of the WD1014 even though $\overline{RCS}$ = 1 since the internal $\overline{RBCS}$ is still active. In a READ operation, the check bytes are recomputed and compared to the recorded check bytes to generate the 4 syndrome bytes. The syndrome bytes are stored internally in the shift registers until the CP is ready to use them. Otherwise, the nonzero syndrome is used by the software algorithm to compute the displacement and the error vector within the bad sector.

To support RLONG and WLONG (L = 1) features of the WD1002-05, shift register strings are used as storage elements. After the last byte of data, the Host can write or read the 4 additional bytes which serve as check bytes for the data transmitted to the buffer. In this mode the feedback terms and the outputs from M.S.B. of the shift registers are disabled so that only data is accepted and stored. This enables the user to alter the check bits / or data to verify the operation of the Error detection logic.

SDH REGISTER

This register can be written into by either the Host or WD1015. The bits are decoded as follows.

BIT	7	6 5	4 3	2 1 0
FUNCTION	CRC + ECC	SECTOR SIZE	DRIVE SELECT	HEAD/DRIVE SELECT

Bit 7 should be set to a 1 whenever a Winchester disk is selected "and" ECC is to be utilized. It must be set to 0 for floppy disks.

Bit 6-5 as shown below specify the sector size.

SDH6	SDH5	SECTOR SIZE IN BYTES
1	1	128
0	0	256
0	1	512
1	0	1024

The decoded bits are used in conjunction with a 3 bit counter which has SC128 as its clock. The falling edge of this input is used to set a counter overflow latch for sector sizes 256, 512 and 1024. The rising edge of this input sets counter overflow latch when the sector size is 128. The counter overflow is available on the output as SBEF and is used internally to set the buffer overflow latch and various other control logic as required by system operation. This counter and associated logic is cleared upon $\overline{MR}$, any new command, or can be directly cleared by CLROVF.

Bits 4-0 are used for drive and head selection and are decoded in the following manner.

Winchester
$HD/\overline{FD} = 1 = \overline{SDH4} + \overline{SDH3} + \overline{SDH4}\cdot\overline{SDH3}$
DSB1 = 1 = SDH3 decoded off chip for one of three
DSB2 = 1 = SDH4 drives.
SDH2-0 = SDH2-0 decoded off chip for one of eight heads.

Floppy
$HD/\overline{FD} = 0 = SDH4\cdot SDH3$
DSB1 = 1 = SDH1 decoded off chip for one of four
DSB2 = 1 = SDH2 drives.
SDH2-0 = Not used.
Side select is controlled by the WD1015 via the WD2797.

COMMAND/ERROR REGISTER

This 8 bit register intercepts and holds the command issued by the Host. When a command is issued:

(a) the sector counter and associated overflow latches are cleared.
(b) the external counters are cleared via CMR
(c) the read command latch is cleared
(d) INTRQ is reset
(e) bit 1 (the long bit) is used by the ECC polynomial to implement the READLONG and WRITELONG command. The CP can also read this latch so that it can execute the command.
(f) WAKEUP is set immediately if the command is a RESTORE, SEEK, or READ. For a WRITE or a FORMAT command, WAUP is set after counter overflow (COVF) occurs or an additional four RAM accesses have occured (SYN4), depending upon the long bit L = 0 or L = 1.

At the completion of a command, this register is reused to hold error information that can be read by the Host. This is necessary since error information from two sources has to be manipulated by the CP and reported to the Host in real time when requested to do so.

ERROR DETECTION LOGIC

The error detection logic consists of an input data buffer and deserializer, two 16-bit shift registers to generate the ECC bytes, and associated control logic consisting of two 3-bit counters and integrated logic.

INPUT DATA BUFFER AND DESERIALIZER

This section is designed to accept a byte of data on the rising edge of $\overline{RE}$ or $\overline{WE}$ under the following conditions:

1. The ECC polynomial is selected as implied by SDH7 = 1.
2. A valid $\overline{RBCS}$ is generated regardless of the counter overflow
3. If the syndrome is to be read by the C.P. after an overflow condition has occurred (i.e., the syndrome is not saved after it has been read by the C.P.).

Valid data presented to the WD1014 device is accepted by the data buffer and the $\overline{ECC}$ shift registers on the rising edge of $\overline{RE}$ or $\overline{WE}$ input strobes. These strobes are synchronized internally by the falling edge of the input clock so that shifting can begin on the rising edge of the clock. Data is serialized and shifted in a 2-bit parallel mode until the internal bit counter reaches the count of 3. This process is repeated for every byte of data until the counter overflow occurs plus an additional 4 bytes have been processed. Under the worst case conditions, a byte of data will be processed within 4 clock cycles after the $\overline{RE}$ or $\overline{WE}$ strobes are terminated.

MULTIPLEXER

The multiplexer is used to channel data to the I/O pins D7-D0 when one of the following conditions occur.

1. The command register is read
2. The error register is read
3. The check bytes are read
4. The syndrome bytes are read

The $\overline{RE}$ strobe gating with the above control signals is designed to keep the hold time on the output data bus to less than 100 n.s. and the data access time to be no more than 200 n.s.

WAKEUP

This signal alerts the external CP that a command has been received and is internally referred to as the busy signal.

WAUP will go high when $\overline{MR}$ is asserted or a command other than WRITE or FORMAT has been received. In the case of a WRITE or FORMAT command WAUP will go high when SBEF = 1 and L = 0, or when an additional four bytes have been accepted by the WD1014 when L = 1.

For proper operation, the READ command latch must be set by the CP whenever that command has been received. Also the Multiple Mode latch is set by the CP in order to execute the same command a multiple number of times. This latch must be reset if executing a READ or a WRITE command only once, or if the last sector of a multiple sector transfer is being processed.

WAKEUP can only be reset by asserting SLEEP.

DATA REQUEST

The true condition of the DRQ latch can oly be sampled by external circuitry if WAUP = 0.

This latch can be set by either the CP, or whenever a WRITE or FORMAT command is written into the WD1014. It is reset by COVF = 1 (SBEF) when L = 0, or until an additional 4 bytes have been accepted by the WD1014 when L = 1.

INTERRUPT REQUEST

Two latches are provided to handle interrupts. The programmed I/O interrupt (PINT) latch is set whenever an interrupt is desired at the start of data transmission to the Host. The DMA interrupt (DINT) latch is set whenever an interrupt is desired at the end of data transmission to the Host.

Both latches are reset when:

1. A $\overline{MR}$ occurs
2. Any command is received
3. The output signal $\overline{HCS}$ is activated.

As in the case of DRQ, the true condition of INTRQ can only be sampled by external circuitry if WAUP = 0.

MISCELLANEOUS CONTROL SIGNALS

The rest of the output signals are purely combinatorial in nature and are best described by Boolean expressions.

1. $\overline{HSC} = \overline{BUSY}.\overline{CSO}.A2.A1.A0.\overline{RE}$
2. $\overline{HBC} = \overline{BUSY}.\overline{CSO}.HSC$
3. $\overline{LUB} = \overline{CS1}.\overline{A2}.A1.A0.\overline{WE}$
4. $\overline{LLB} = \overline{CS1}.\overline{A2}.A1.\overline{A0}.\overline{WE}$
5. $\overline{RCS} = \overline{COVF}(\overline{CSO}.\overline{A2}.\overline{A1}.\overline{A0} + \overline{BCS})$
6. $\overline{HDCS} = (\overline{BUSY}.A2.A1.A0. + \overline{BUSY}..\overline{A2}.\overline{A1}.\overline{RE} + \overline{CSO})$

$\overline{HDCS}$ is active only if the Host is not accessing the error, status or the command registers of the WD1010 device, and $\overline{CSO}$ is asserted.

7. $\overline{CINC} = \overline{COVF}.\overline{RSC}(\overline{WE} + \overline{RE})$
8. CMR = $\overline{MR}$ + CST where CST = $\overline{BUSY}.\overline{CSO}$ .A2.A1.A0.$\overline{WE}$(Any cmd written)
9. SBEF = COVF

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Ambient Temperatures
under bias . . . . . 0°C (32°F) to 70°C (158°F)

Voltage on any pin
with respect to V_{SS} . . . . . -0.2V to + 7.0V

Power dissipation . . . . . 1.5 Watt

STORAGE TEMPERATURE

Plastic . . . . . -55°C(-67°F) to + 125°C(257°F)

Ceramic . . . . . -55°C(-67°F) to + 150°C(302°F)

NOTE:

Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

TABLE 1. DC Electrical Characteristics T_A = 0°C (32°F) to 70°C (158°F), V_{CC} = +5V ±.25V, V_{SS} = 0V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
VIL	Input Low Voltage	-0.2		0.8	V	
VIH	Input High Voltage	2.0			V	
VOL	Output Low Voltage			.04	V	I_{OL} = 1.6 mA
VOH	Output High Voltage	2.4			V	I_{OH} = -100 mA
VCC	Supply Voltage	4.75	5.0	5.25	V	
ICC	Supply Current		200	250	mA	All outputs open

TIMING PARAMETERS

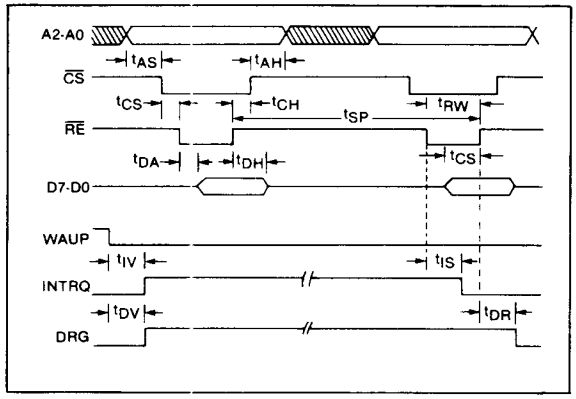


FIGURE 1. DATA READ CYCLE

TABLE 2. DATA READ CYCLE TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
f_{CP}	Input Clock Freq.		6.0	5.0	MHZ	
t_{AS}	Address Setup to $\overline{CS}$	100	70		nS	
t_{AH}	Address Hold from $\overline{CS}$	50	20		nS	
t_{CS}	Chip Selects Setup to $\overline{RE}$	100	70		nS	
t_{CH}	Chip Selects Hold from $\overline{RE}$	50	20		nS	
t_{RE}	$\overline{RE}$ pulsewidth	150	120		nS	
t_{SP}	$\overline{RE}$ Strobes period (rising edge)	4			CP	
t_{DA}	Data Access after $\overline{RE}$ active		100	150	nS	
t_{DH}	Data Hold after $\overline{RE}$ inactive		50	100	nS	reading
t_{DS}	Data Setup to $\overline{RE}$ inactive	50	10		nS	
t_{IV}	Interrupt Request valid		50 200	100 250	nS nS	Prog. I/O INT DMA INT
t_{IS}	INTRQ Reset		100	200	nS	
t_{DV}	Data Request Valid		50	100	nS	
t_{DR}	DRQ Reset		100	200	nS	

AC ELECTRICAL CHARACTERISTICS

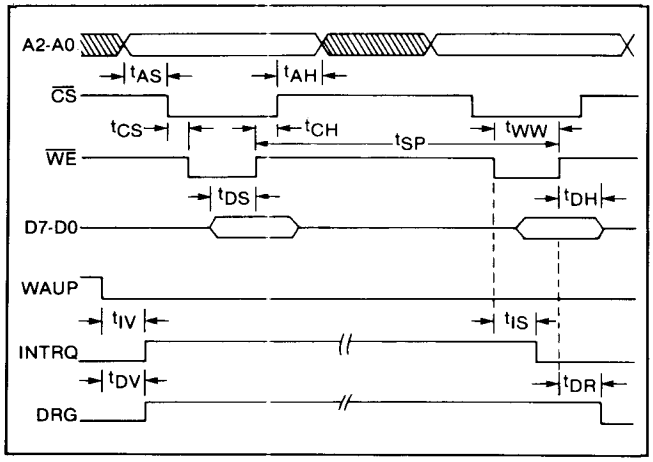


FIGURE 2. DATA WRITE CYCLE

TABLE 3. DATA WRITE CYCLE TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
f_{CP}	Input Clock Freq.		6.0	5.0	MHZ	
t_{AS}	Address Setup to $\overline{CS}$	100	70		nS	
t_{AH}	Address Hold from $\overline{CS}$	50	20		nS	
t_{CS}	Chip Selects Setup to $\overline{WE}$	100	70		nS	
t_{CH}	Chip Selects Hold from $\overline{WE}$	50	20		nS	
t_{WE}	$\overline{WE}$ pulsewidth	150	120		nS	
t_{SP}	$\overline{WE}$ Strobes period (rising edge)	4			CP	
t_{DHW}	Data Hold after $\overline{WE}$ inactive	0	30		nS	writing
t_{DS}	Data Setup to $\overline{WE}$ inactive	50	10		nS	
t_{IV}	Interrupt Request valid		50	100	nS	Prog. I/O INT
		50	200	250	nS	DMA INT
t_{IS}	INTRQ Reset		100	200	nS	
t_{DV}	Data Request Valid		50	100	nS	
t_{DR}	DRQ Reset		100	200	nS	

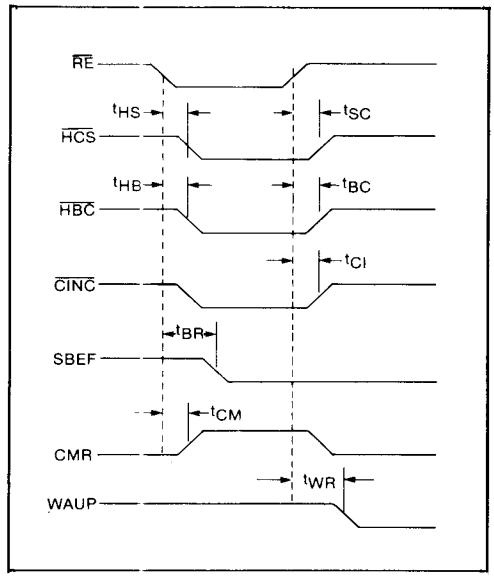


FIGURE 3. OUTPUT SIGNALS W.R.T. $\overline{RE}$

TABLE 4. OUTPUT SIGNAL (W.R.T.) $\overline{RE}$ TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{CI}	$\overline{RE}$ to Count Increm.		50	100	nS	rising edges
t_{HS}	$\overline{RE}$ to Status Strobe		130	200	nS	
t_{SC}	$\overline{RE}$ to $\overline{HSC}$ inactive		130	200	nS	
t_{HB}	$\overline{CS0}$ to Host bus str		70	200	nS	active if $\overline{HSC}$ off
t_{BC}	$\overline{CS0}$ to $\overline{HBC}$ inact.		80	200	nS	active if $\overline{HSC}$ off
t_{BR}	$\overline{RE}$ to cir SBEF		250	300	nS	using CLROVF strobe
t_{CM}	$\overline{RE}$ to counter reset		200	300	nS	using CLROVF strobe
t_{WR}	$\overline{RE}$ to WAUP reset		100	200	nS	using SLEEP strobe

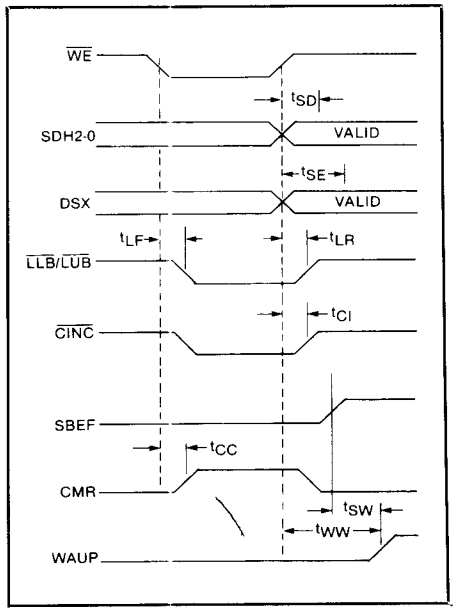


FIGURE 4. OUTPUT SIGNALS W.R.T. $\overline{WE}$

TABLE 5. OUTPUT SIGNAL (W.R.T.) $\overline{WE}$ TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{SD}	$\overline{WE}$ Inactive to SDHX output		150	200	nS	
t_{SE}	$\overline{WE}$ Inactive to DSX output		175	200	nS	
t_{LF}	$\overline{WE}$ to $\overline{LLB}/\overline{LUB}$		70	150	nS	falling edges
t_{LR}	$\overline{WE}$ to $\overline{LLB}/\overline{LUB}$		80	150	nS	rising edges
t_{CI}	$\overline{WE}$ to Count Increm.		50	100	nS	rising edges
t_{CC}	$\overline{WE}$ to Counter Reset		150	200	nS	
t_{SW}	SBEF to WAUP set		50	200	nS	
t_{WW}	$\overline{WE}$ to WAUP set		175	200	nS	Command written

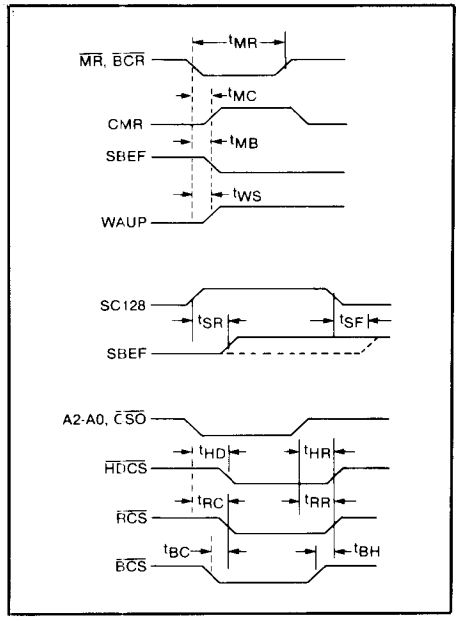


FIGURE 5. MISCELLANEOUS TIMINGS

TABLE 6. MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
t_{MR}	Master reset/Buffer counter reset width	100	50		nS	
t_{MC}	$\overline{MR}/\overline{BCR}$ to counter reset		60	100	nS	
t_{MB}	$\overline{MR}/\overline{BCR}$ to SBEF rst		130	200	nS	
t_{WS}	$\overline{MR}$ to WAUP reset		100	200	nS	$\overline{BCR}$ has no effect
t_{SR}	Rising Edge of SC128 to SBEF		100	200	nS	128 byte sector
t_{SF}	Falling Edge of SC128 to SBEF		150	200	nS	all other sectors
t_{HD}	$\overline{CS0}$ to $\overline{HDCS}$		70	150	nS	(or address lines)
t_{HR}	$\overline{CS0}$ to $\overline{HDCS}$ rising to $\overline{CMR}$		80	150	nS	
t_{RC}	$\overline{CS0}$ to $\overline{RCS}$ active		90	150	nS	(or address lines)
t_{RR}	$\overline{CS0}$ to $\overline{RCS}$ high		100	150	nS	
t_{BC}	$\overline{BCS}$ to $\overline{RCS}$ active		50	100	nS	
t_{BH}	$\overline{BCS}$ to $\overline{RCS}$ high		60	100	nS	