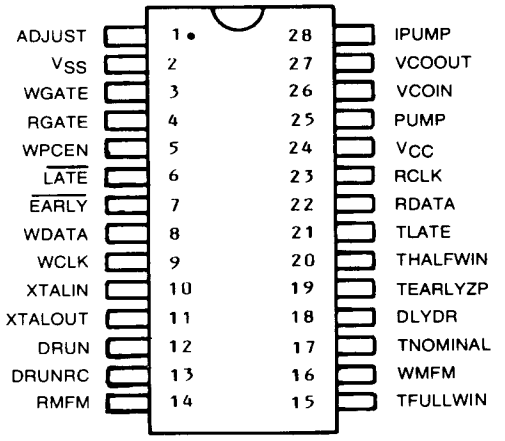
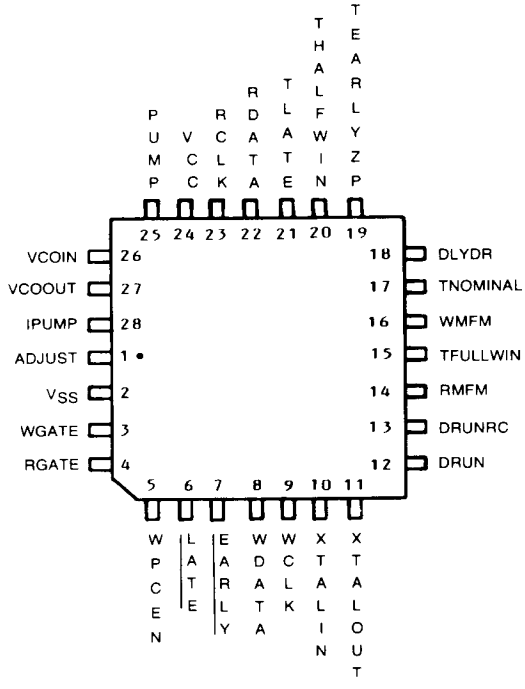
WD10C20-05 Self-Adjusting Data Separator

FEATURES

- PROCESSES ALL SENSITIVE READ/WRITE DATA SIGNALS
- CMOS TECHNOLOGY
- DESIGNED FOR ST506/ST412 AND WD1010/ WD2010 INTERFACE
- HIGHLY STABLE LC TYPE VOLTAGE CONTROLLED OSCILLATOR
- SELF ADJUSTING VCO COMPENSATES FOR COMPONENT, TEMPERATURE, VOLTAGE, AND AGING VARIATIONS
- FREQUENCY DETECTION ON CRYSTAL REFERENCE AND DATA SYNCHRONIZATION FIELD, ELIMINATES 180 DEGREE LOCK DUE TO DRIVE ASYMMETRY, AND ELIMINATES HARMONIC LOCK FROM WRITE SPLICES
- ZERO PHASE STARTUP PROVIDES FASTER, MORE PREDICATABLE LOCK ACQUISITION
- LOCKS TO CRYSTAL REFERENCE WHILE IDLE
- DUAL GAIN: HIGH FOR FASTER ACQUISITION
  LOW FOR MORE JITTER REJECTION WHILE TRACKING
- EXTERNAL PUMP CURRENT CONTROL
- AVAILABLE IN 28-PIN DIP OR QSM PACKAGE
- INTEGRATED CRYSTAL OSCILLATOR
- ACCOMMODATES OTHER DATA RATES THROUGH SELECTION OF EXTERNAL COMPONENTS





PIN DESIGNATION

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DESCRIPTION

The WD10C20-05 is an LSI device implemented in 3 micron high-speed CMOS, designed to be compatible with the WD1010 and WD2010 Winchester Disk Controllers and ST506/ST412 disk drives. In a typical application, it handles all sensitive read/write signals between a WD1010/WD2010 and the data drivers/receivers. Read data corresponds to previous write data, with added phase, frequency, and write splice noise. The WD10C20-05 removes these sources of noise and presents a clean, digital read signal to the WD1010/WD2010.

While reading, the WD10C20-05 performs phase-locked loop data synchronization on data read from the drive. An on-board Sync Field detector automatically switches the PLL from the stable crystal reference to the read data. Zero-phase start-up results when the VCO is halted and restarted in phase with the data to eliminate initial acquisition in the wrong frequency direction. Frequency-phase detection is used at the beginning of the Sync Field to quickly and reliably acquire lock to the data. Use of this technique eliminates susceptibility to harmonics and asymmetry. The WD10C20-05 then switches to phase-only detection to complete the phase acquisition before the end of the Synch Field and to enable tracking of random MFM read data. When switching to phase detection, the WD10C20-05 reduces the error amplifier gain for better rejection of drive jitter. A precisely aligned detector samples the data at twice the underlying data rate to remove the phase jitter. The regenerated signal, along with a fixed-phase synchronous clock, are output to the WD1010/WD2010 digital circuits.

While writing, the WD10C20-05 conditions the write data to the drive. MFM data from the WD1010/WD2010 is precisely clocked, with a signal at twice the data frequency, to minimize digital phase noise. If precompensation is enabled, early, nominal, and late taps on an external delay line are multiplexed through matched delay paths to produce synchronized, precompensated write data, which is sent directly to the drive's write circuits.

The WD10C20-05 is designed to work at the 5 Mbit/sec data rate of the ST506/ST412 interface. Other data rates may be accommodated through the proper selection of external components.

NOTE: To assure reliable operation of the WD10C20-05, it is recommended that the WD10C20-05 KIT, number 77-000014 be used. If the user elects to not use the kit, the external components as shown in Figure 1, must be selected from the parts listed in the WD10C20-05 Application Note. The placement of these components must conform to the layout illustrated in the Application Note. (The Application Note is available through your Western Digital field representative.)

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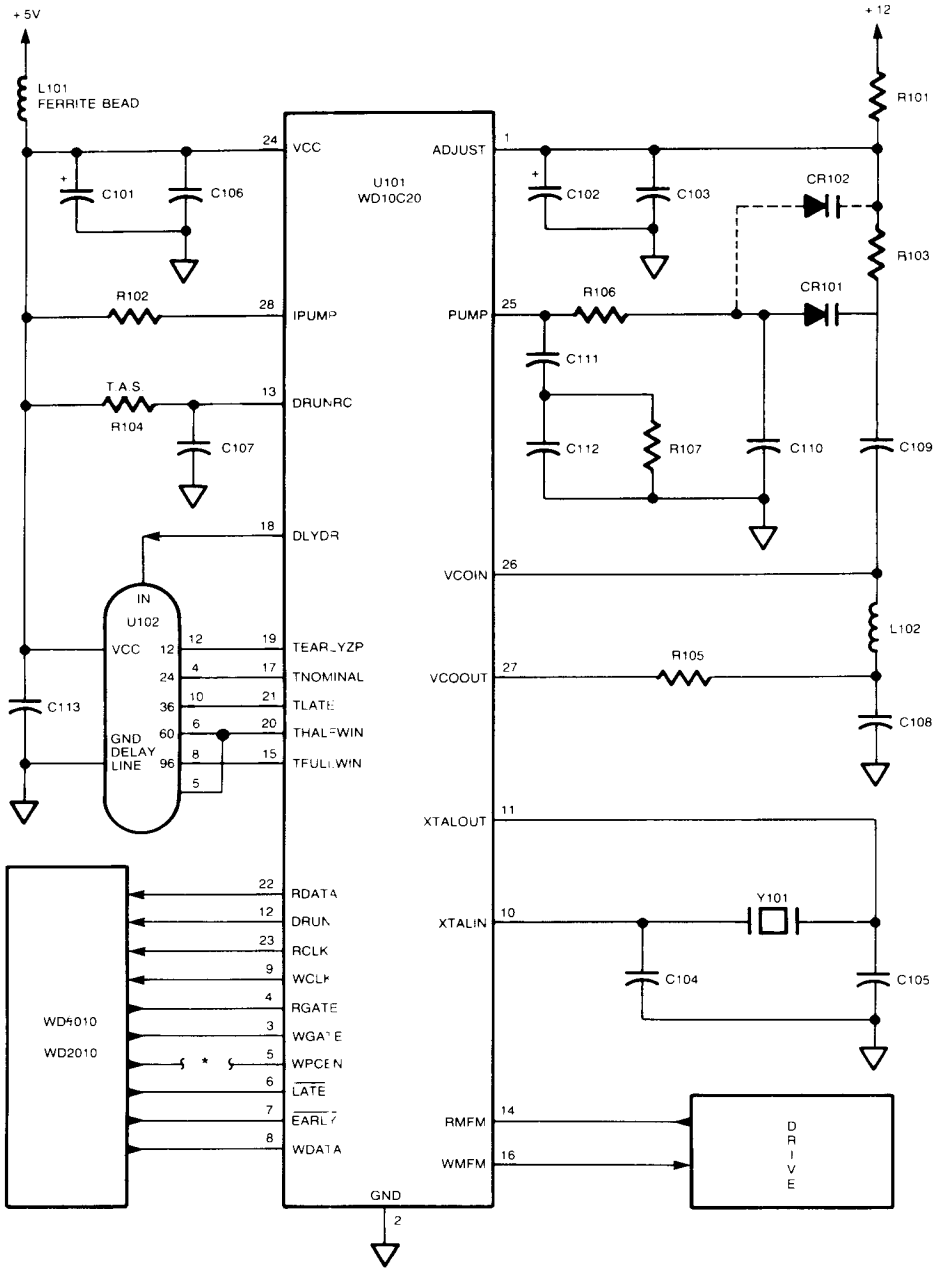

*RWC CONNNECTS TO WPCEN IF REDUCED WRITE CURRENT IS TO START AT THE SAME TIME AS WRITE PRECOMP. THE WD1002S-WX2 USES LS/DIR/WPC.

FIGURE 1. EXTERNAL COMPONENTS

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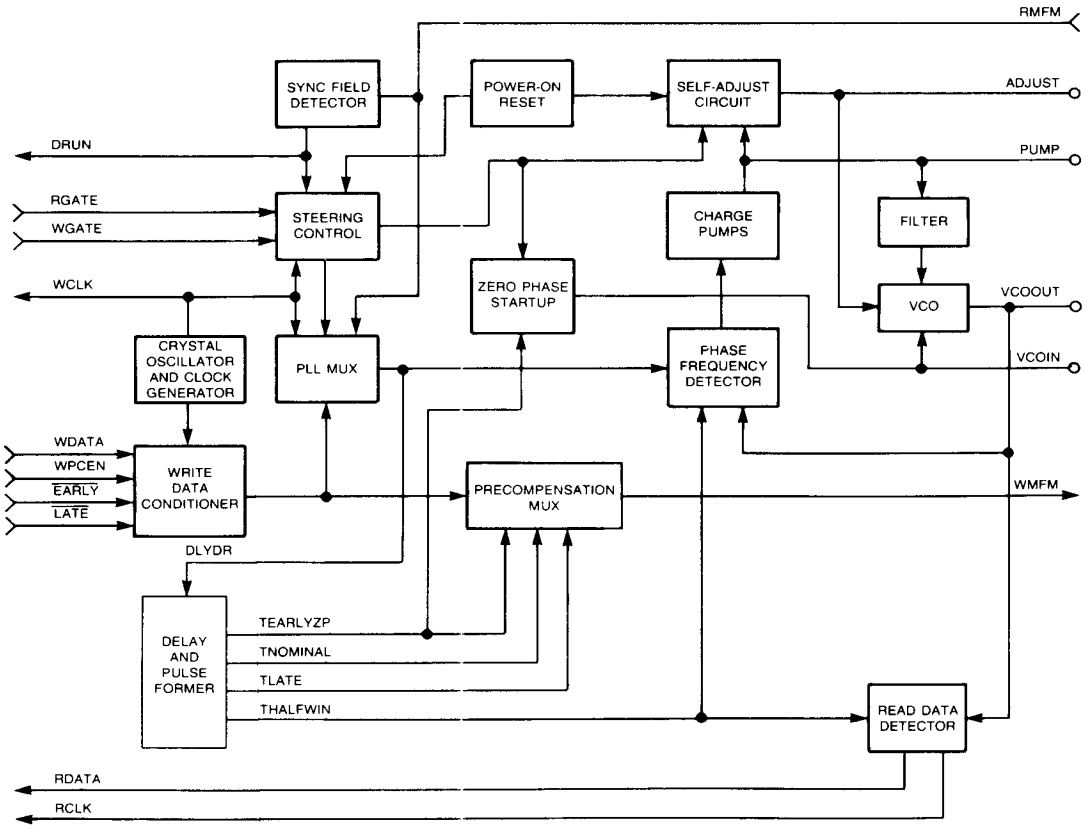

FIGURE 2. WD10C20 BLOCK DIAGRAM

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PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	ADJUST	ADJUST	O	Provides self calibration of the PLL.
2	VSS	GROUND		
3	WGATE	WRITE GATE	I	WGATE is asserted when the controller writes on the disk.
4	RGATE	READ GATE	I	RGATE is asserted when the controller intends to read from the disk. RGATE causes the WD10C20-05 to remain locked onto the incoming data stream.
5	WPCEN	WRITE PRECOMP ENABLE	I	WPCEN is asserted to enable the $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ signals from the controller. WPCEN may be connected to the Reduce Write Current (RWC) available from the WD1010/WD2010 if Write Precomp is to occur at the same time as the Reduced Write Current, or to an independent source if they start at different times.
6	$\overline{\text{LATE}}$	$\overline{\text{LATE}}$	I	Asserted by the Controller to delay the writing of a bit to the disk.
7	$\overline{\text{EARLY}}$	$\overline{\text{EARLY}}$	I	Asserted by the Controller to advance the writing of a bit to the disk.
8	WDATA	WRITE DATA	I	Non-Synchronized and Non-Precompensated MFM data from the controller to be written on the disk via WMFM.
9	WCLK	WRITE CLOCK	O	WCLK is equal to XTALIN ÷ 2 and is used by the controller to generate the data to be written.
10	XTALIN	XTALIN	I	XTALIN is a crystal controlled oscillator input used by a number of internal control functions. Divided by 2 it develops WCLK. XTALIN may also be driven by an external driver in which case XTALOUT is left open. The input level of this pin is not TTL and must be guaranteed by the clock source.
11	XTALOUT	XTALOUT	O	XTALOUT is the crystal controlled oscillator output. When an external frequency source is used, this pin is left open.
12	DRUN	DATA RUN	O	DRUN is a signal that discriminates between frequencies on RMFM. It goes low for low frequencies and high for high frequencies. Its nominal threshold is set to 1-3/8 bit times using DRUNRC. DRUN remains asserted for a continuous stream of one's or zero's. ie: Sync Field.
13	DRUNRC	DRUNRC	I	Connected to an external RC circuit for the generation of DRUN.
14	RMFM	READ MFM DATA	I	MFM Data received from the drive. A nominal 4K ohm internal pullup resistor allows tri-state multiplexing of the driver's data receivers.
15	TFULLWIN	TFULLWINDOW	I	Delay line tap for generating full window RMFM pulses.
16	WMFM	WRITE MFM DATA	O	Preconditioned WDATA ready to be written on the disk. WMFM is held low when WGATE is low.
17	TNOMINAL	TNOMINAL	I	Delay line tap for uncompensated write data.

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PIN DESCRIPTION (Continued)

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
18	DYLDR	DELAY LINE DRIVER	O	Drives an external delay line.
19	TEARLYZP	TEARLY ZERO PHASE TIMING	I	Delay line tap for early precompensated write data and for zero phase startup of the VCO.
20	THALFWIN	THALFWINDOW	I	Delay line tap for generating the enable phase delay when in phase detection mode.
21	TLATE	TLATE	I	Delay line tap for late precompensated write data.
22	RDATA	READ DATA	O	RDATA is RMFM synchronized to RCLK. The clock is removed from the RMFM by the controller.
23	RCLK	READ CLOCK	O	RCLK is equal to one half of VCO and is synchronized to RDATA during a read operation and to WCLK while in an idle state.
24	VCC	POWER SUPPLY	I	+5V Power Supply.
25	PUMP	PUMP	I/O	Charge PUMP to the PLL filter. Also a voltage input to the self-adjust sensing circuitry.
26	VCOIN	VOLTAGE CONTROL OSCILLATOR INPUT	I	Input to the VCO gain stage. VCOIN is clamped low, and then released during zero phase startup.
27	VCOOUT	VOLTAGE CONTROL OSCILLATOR OUTPUT	O	Output from the VCO gain stage.
28	IPUMP	IPUMP	I	An external resistor connected to IPUMP establishes the magnitude of the charge pump current and ADJUST current.

ARCHITECTURE

The WD10C20-05, with the necessay external components, provides the data interface between the WD1010 or WD2010 and an ST506/ST412 compatible drive. There are eight major functional sections within the WD10C20-05:

- Synchronized Field Detector
- Steering Control
- Phase-locked Loop (PLL)
  - Phase-frequency Detector
  - Charge Pumps
  - Filter
  - Voltage Controller Oscillator (VCO)
  - Zero Phase Startup Circuit
  - Self Adjustment Circuit
- Read Data Detector
- Crystal Oscillator
- Write Data Conditioner
- Delay And Pulse Former
- Power-on Reset

SYNCHRONIZATION FIELD DETECTOR

The Synchronization Field Detector discriminates between the 00's of a Synchronization Field and the low frequency data immediately preceding these fields. The criterion used is pulse period discrimination on the RMFM data. The external resistor and capacitor connected to DRUNRC sets the nominal detection threshold of 1-3/8 bit times. DRUN goes low for long periods and high for short periods.

STEERING CONTROL

This logic controls the sequencing of events when the WD10C20-05 is switching between read, write and idle modes. When switching, the Steering Control disables the Phase-Frequency Detector and Charge Pumps, switches the MUX source, invokes zero-phase startup, selects the velocity lock mode of the Phase-Frequency Detector, and high gain on the Charge Pump. After the zero-phase startup is complete, the Phase-Frequency Detector and Charge pumps are enabled. If the device is in read or write mode, after four byte times the Steering Control switches to phase detection, and the charge pumps are set to low gain.

PHASE-LOCKED LOOP

Phase-Frequency Detector

The Phase-Frequency Detector operates in one of two modes: velocity lock mode or phase-only detection.

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Velocity lock mode is used for acquisition when the PLL is switched to read or write data or when the PLL is following the reference crystal oscillator.

The Steering Control logic switches to the Phase-only mode when frequency and phase acquisition is nearly complete. Internal delay paths have been carefully matched to minimize introduction of a phase error due to switching. The phase-only mode must be used to lock to the MFM following the Sync Field, since that contains the three MFM frequencies.

In either mode, the Phase-Frequency detector converts a phase difference between the VCO and the input to a pulse width equal to the phase difference. The polarity of the phase error determines whether a signal is directed to the pump up or pump down circuitry in the Charge Pump section.

Charge Pumps

The Charge Pump circuit converts the widths received from the Phase-Frequency Detector to proportional amounts of charge, into or out of the filter. The gain of the Charge Pumps is set by the input current of the IPUMP signal. This current is set by an external resistor connected to the VCC.

Filter

The Filter converts the current pulses from the Charge Pumps to a voltage ouptut to the VCO. It also peforms the sample-and-hold function necessary for an edge locked PLL, and is also necessary during the zero phase startup period. As shown in Figure 1, one of the filter's capacitors (C110) is also part of the VCO's series resonant oscillator.

The filter must meet the specific requirements of acquisition time, capture range, and jitter ejection, and within the context of its effect on VCO operation. The filter functions to block high frequency signals due to RMFM read data jitter, and passes the low frequency signals of the RMFM.

Voltage Controlled Oscillator

The VCO is a series resonant LC oscillator. The active gain element that provides the energy to sustain oscillation is within the WD10C20-05, between the VCOIN and VCOOUT pins. An inexpensive varactor controls and tunes the VCO. The filter connects to the anode of the varactor and provides the voltage for loop operation of the PLL. Higher voltages at the VCO input correspond to lower frequencies, and lower voltages correspond to higher frequencies. The self-adjustment circuit connects to the cathode of the varactor. The voltage bias at this point determines the location of the VCO's V-F characteristic curve, and is set for a favorable VCO input voltage at the nominal frequency of the VCO.

Zero Phase Startup Circuit

The VCOIN connects to the Zero Phase Startup Circuit, which contains the logic necessary to turn a clamp on or off. This clamp, in turn, enables or disables the VCO gain stage. When the WD10C20-05 changes the PLL input signal, the clamp is turned on for a minimum of one input data period. This stops the VCO gain and removes the AC energy from the passive VCO components. The VCO is now in a known state, and the time between the release of the clamp and the time the first edge of the VCO reaches the Phase Frequency Detector can be predicted. This event is made to coincide with the arrival of a data pulse by the delay between TEARLYZP and THALFWIN.

Self Adjustment Circuit

The Self Adjustment Circuit (SAC) serves to slowly maintain the VCO's input voltage near the sense level. It performs compensation for component variations in much the same way as manual adjustments, as well as dynamic variations such as temperature, voltage and aging. Another advantage of this circuit is the heavy RC filtering of the + 12 volt supply. The SAC tunes the VCO so that its nominal output frequency of twice the data rate corresponds to an input voltage favorable to the Charge Pumps. This voltage is approximately half of the VCC, and centers the capture range. The PUMP signal connects to an internal comparator and senses the VCO input voltage to determine whether it is above or below the threshold voltage (VSENSE).

The comparator is sampled at a low frequency derived from the crystal. The output is used as the up / down control to a six-bit counter. At power-on, this counter is set to half scale. The least significant two bits are for noise immunity only. The most significant four bits connect to a digital-to-analog converter (DAC) that controls the current-sinking ability of the ADJUST signal. To convert the ADJUST signal current to a voltage, it is connected externally through a resistor to the + 12V. To filter the DAC steps and transients, the ADJUST is connected to two capacitors. A resistor from the ADJUST signal to the cathode of the VCO varactor completes the circuit. Refer to Figure 1.

READ DATA DETECTOR

The Read Data Detector produces RCLK and RDATA. RCLK is a square wave equal to one half of the VCO frequency. During data tracking, RCLK mirrors the slowly varying frequency of the RMFM. RDATA is a regenerated form of the RMFM, with the jitter removed and one-half bit-time pulse widths, and is exactly synchronous with RCLK. RCLK edges occur nominally in the center of RDATA to allow sufficient setup and hold time for the digital circuits in the WD1010 / WD2010 using these signals.

CRYSTAL OSCILLATOR

The Crystal Oscillator is designed to operate in the parallel resonant mode, with an external crystal and two capacitors. It generates the WCLK signal used externally. Internally, various divisions of it are used by the Write Data Conditioner, PLL, and SAC.

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When an externally generated clock is desired, the crystal and capacitors are omitted. The XTALIN pin is connected to the clock source, and XTALOUT is left disconnected. The input levels of XTALIN are not TTL and must be guaranteed by the clock source.

WRITE DATA CONDITIONER

The Write Data Conditioner samples and precisely synchronizes WDATA, EARLY, and LATE on the leading and trailing edges of WCLK. When WGATE is asserted, the DLYDR signal is a direct derivative of WDATA and is connected to the input of the delay line. It returns to the WD10C20-05 via the TEARLYZP, TNOMINAL, and TLATE input signals. When WPCEN is de- asserted, WMFM follows the TNOMINAL signal. When WPCEN is asserted, the EARLY and LATE signals select the TEARLYZP and TLATE inputs, respectively. The differential delay between TEARLYZP and TNOMINAL at the delay line defines the amount of early precompensation, and similarly, the differential delay between TNOMINAL to TLATE defines the amount of late precompensation.

When WGATE is asserted, one of the initial MFM pulses is suppressed to create an interval of two bit times. This ensures that DRUN will go low at the beginning of a Sync Field preceding a data field, so that zero phase startup and velocity lock are executed properly. When WGATE is de-asserted. WMFM is held low.

DELAY AND PULSE FORMER

The Delay And Pulse Former includes the external delay line as well as logic internal to the WD10C20-05. In response to rising edges, it produces positive pulses slightly longer than one detection window, which is half of one bit time. The taps are also used for write precompensation, zero-phase startup, and defining the enable window for phase detection. Depending on the mode of operation, its input is either RMFM, synchronized WDATA, or WCLK.

POWER-ON RESET

This integrated function is used to reliably set flip-flops to a predictable state during the application of the VCC. It is used by the Steering Control and SAC sections.

DATA SEPARATOR CIRCUIT PERFORMANCE SPECIFICATIONS

The following specifications apply when the external components are selected as specified and operate within the following ranges:

$V_{CC} = +5V \pm .25V$ with $\leq$ 100 mV ripple, 0 to 30 KHz
$+12V = +12V \pm 1.2V$ with $\leq$ 200 mV ripple, 0 to 30 KHz
Temperature = 0° to 70°C (32° to 158°F)

PHASE-LOCKED LOOP:

• Acquisition Time	< 12.8 usec (16 usec from DRUN high)	
• Capture Range	> ± 2.2% (± 1% drive ± .1% crystal Osc.)	
• Jitter Rejection	>40 db at 2.5 MHz	
• Damping Factor	min .7 typ. 1 max 1.4 Velocity Lock	
	min .5 typ. .7 max 1.1 Phase Detection	
• KD Error Amplifier Gain	min 2 mA	Velocity Lock
	typ 6 mA	Operating Range
	max 10 mA	VSENSE ± 1060 mv
	min 1 mA	Phase Detection
	typ 4.3 mA	Operating Range
	max 6.8 mA	VSENSE ± 950 mV
• Error Amplifier Balance Ratio	max 2:1	Phase Detection Operating Range VSENSE ± 950 mV Phase: ± 5 to ± 40 nsec
• Ko VCO Gain	min 4.5% per volt	
	typ 5% per volt	
	max 7.5% per volt	

FREQUENCY DETECTOR

DRUN must be high in response to RMFM rising edge to rising edge periods less than 250 nsec. DRUN must be low for periods greater than 300 nsec.

CRYSTAL OSCILLATOR

The operational frequency must be within ± .1% of 10 MHz.

PHASE DETECTOR/CHARGE PUMPS

Phase Decision Points

While in the phase detection mode, the phase difference from null (zero pump current) to the decision points must be no less than ± 40 nsec.

VCO GAIN

Over the VCO input voltage range, VSENSE nominal ± 1060 mV, the VCO gain must be within the range of 4.5% to 7.5% per volt. There must be no interruptions in its characteristic V-F curve over the input voltage range.

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WD10C20-05 ELECTRICAL CHARCTERISTICS

MAXIMUM RATINGS

V_{CC} with respect to V_{SS} ..... +5.5 Volts
Max Voltage range on any pin ..... -0.5V to 0.5V > V_{CC}
(except ADJUST) with respect to V_{SS}
Max Voltage Range on ADJUST with respect to V_{SS} ..... -0.5V to +13.2V
Operating Temperature ..... 0°C(32°F) to 70°C(158°F)
Storage Temperature ..... -65°C(-85°F) to 150°C(302°F)

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics

DC OPERATING CHARACTERISTICS
T_A = 0°C (32°F) to 70°C (158°F)
V_{CC} = +5V ±.25V

Input signals:
TEARLYZP, TNOMINAL, TLATE, THALFWIN, TFULLWIN, RGATE,
WGATE, WPCEN, WDATA, $\overline{\text{EARLY}}$, $\overline{\text{LATE}}$, RMFM

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
V_{IH}	Voltage Input High	3.0			V	
V_{IL}	Voltage Input Low			.8	V	

Input signals:
TEARLYZP, TNOMINAL, TLATE, THALFWIN, TFULLWIN,
RGATE, WGATE, XTALIN, VCOIN (Clamp off)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
I_{IN}	Input leakage			±10	μA	V_{IN} = GND to V_{CC}

Input signals: WDATA, $\overline{\text{EARLY}}$, $\overline{\text{LATE}}$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
I_{IH}	Current Input High			+10	μA	V_{IH} = 3.4 V*
I_{IL}	Current Input Low			-4	mA	V_{IL} = .45 V*

Input signal: WPCEN

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
I_{IH}	Current Input High			+10	μA	V_{IH} = 3.4 V*
I_{IL}	Current Input Low			-2	mA	V_{IL} = .4 V*

*These inputs may or may not have an internal pullup resistor.
In either case, if I_{IH} and I_{IL} meet these specs, the inputs will be driven correctly.

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Input signal: RMFM

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
I_{IH}	Current Input High			0	mA	V_{IH} = 3.4 V
I_{IL}	Current Input Low			-2.5	mA	V_{IL} = .4 V Internal pullup resistor

Input signal: XTALIN

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
V_{IH}	Voltage Input High	3.6			V	
V_{IL}	Voltage Input Low			.6	V	

Output signals: WCLK**, WMFM, DLYDR

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
V_{OH}	Voltage Output High	2.4			V	I_{OH} = -1 mA
V_{OL}	Voltage Output Low			.4	V	I_{OL} = 4 mA
T_{RISE}	Rise Time .8 to 2.0 V			10	nsec	CL = 30 pf
T_{FALL}	Fall Time 2.0 to .8 V			10	nsec	CL = 30 pf

Output signal: WCLK**

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
V_{OH}	Voltage Output High	4.6			V	I_{OH} = -100 μA
V_{OL}	Voltage Output Low			.2	V	I_{OL} = 1 mA
T_{RISE}	Rise Time .9 to 4.2 V			30	nsec	CL = 30 pf
T_{FALL}	Fall Time 4.2 to .9 V			30	nsec	CL = 30 pf

**WCLK has two requirements. It must be able to drive special WD1010 / WD2010 inputs, as well as a buffer at TTL levels. In any application, the total capacitance of the WD1010 / WD2010, buffer, and PC board, must not be more than 30 pf. The total input current of the WD1010 / WD2010 and buffer at the different input voltages must not exceed the above specification.

Output signals: RCLK, RDATA, DRUN

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
V_{OH}	Voltage Output High	4.65			V	I_{OH} = -20 μA
V_{OL}	Voltage Output Low			.2	V	I_{OL} = 20 μA
T_{RISE}	Rise Time .9 to 4.2 V			30	nsec	CL = 20 pf
T_{FALL}	Fall Time 4.2 to .9 V			30	nsec	CL = 20 pf

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Self Adjust, Pump, and Power

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
V_S	VSENSE Threshold		2.4		V	
I_A	ACQUISITION PUMP Current		±6		mA	3.57K on IPUMP***
I_T	TRACKING PUMP Current		±4.5		mA	3.57K on IPUMP***
I_{JMX}	ADJUST Max Current	.4	.6	1.0	mA	3.57K on IPUMP***
I_{JMN}	ADJUST Min Current			±10	μA	
I_{CC}	Power Supply Current		40		mA	3.57K on IPUMP, 5MHz

***Depending upon the application, there are specific requirements upon the pump currents and their relationship to VSENSE. This document is written for 5 Mbit/sec, WD1010/WD2010, ST506/ST412 drive.

AC OPERATING CHARACTERISTICS

Timing on signals RDATA, RCLK, WCLK, and DRUN are measured at the voltage halfway between the WD1010/WD2010's VIH and VIL: 2.55 Volts. All other signals are measured from the 1.4 volt transition. All timing is measured with the load capacitance, CL = 50 pf.

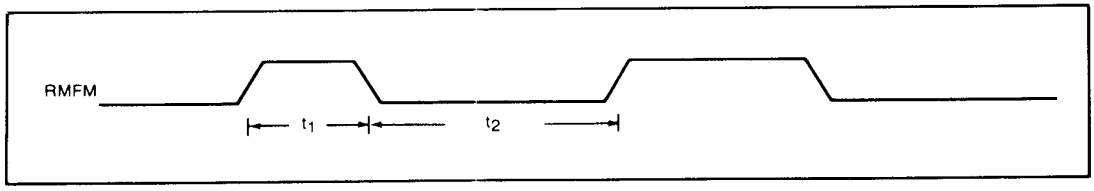

FIGURE 3. DISK DRIVE READ DATA, PULSE FORMING

TABLE 1. DISK DRIVE READ DATA, PULSE FORMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
t_1	RMFM Pulse Width High	20		150	nsec	
t_2	RMFM Pulse Width Low	25			nsec	

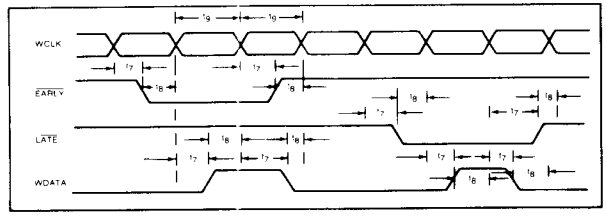

FIGURE 4. WRITE SETUP/OLD

TABLE 2. WRITE SETUP/HOLD

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
t_7	Hold Time	5			nsec	
t_8	Setup Time	20			nsec	
t_9	WCLK Pulse Width	95		105	nsec	

Setup and Hold time is independent of the application of the WD10C20-05.

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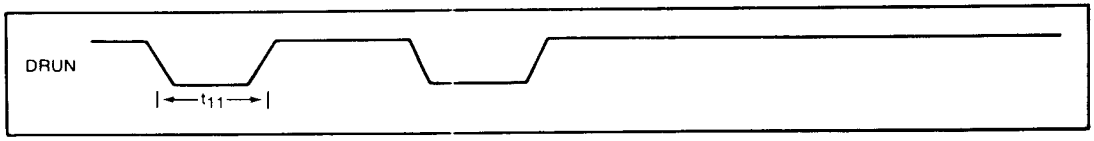

FIGURE 5. DRUN

TABLE 3. DRUN

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
t_{11}	DRUN Low Pulse Width	30			nsec	*

*No requirement on DRUN pulse width high

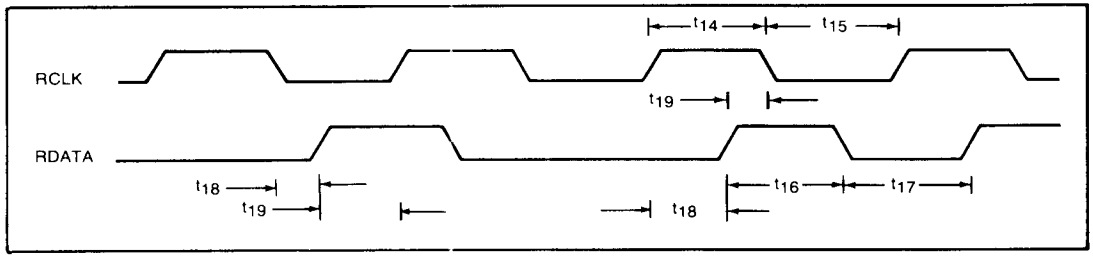

FIGURE 6. RCLK, RDATA TIMING

TABLE 4. RCLK, RDATA TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
t_{14}	RCLK High Pulse Width	93		108	nsec	
t_{15}	RCLK Low Pulse Width	93		108	nsec	
t_{16}	RDATA High Pulse Width	93		108	nsec	
t_{17}	RDATA Low Pulse Width	93		108	nsec	
t_{18}	RCLK Edge to RDATA Rising Edge	30			nsec	Max is implicit in t_{19}min
t_{19}	RDATA Rising Edge To RCLK Edge	30			nsec	Max is implicit in t_{18}min

t_{14} and t_{15} each define an MFM detection window. The rising edge of RDATA must occur within the window. $t_{14} + t_{15}$ = the current bit cell time.

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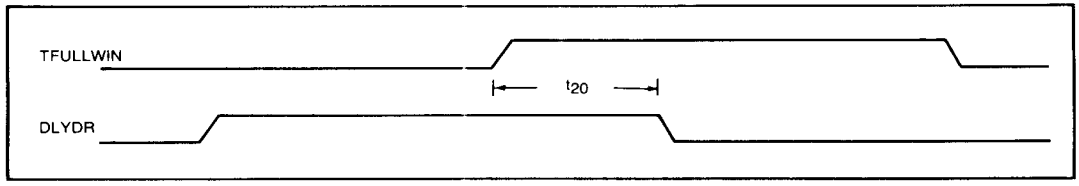
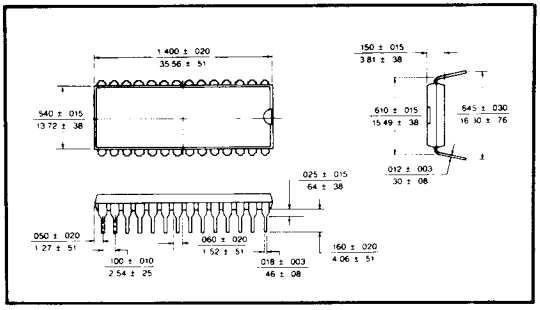


FIGURE 7. DLYDR, TFULLWIN TIMING

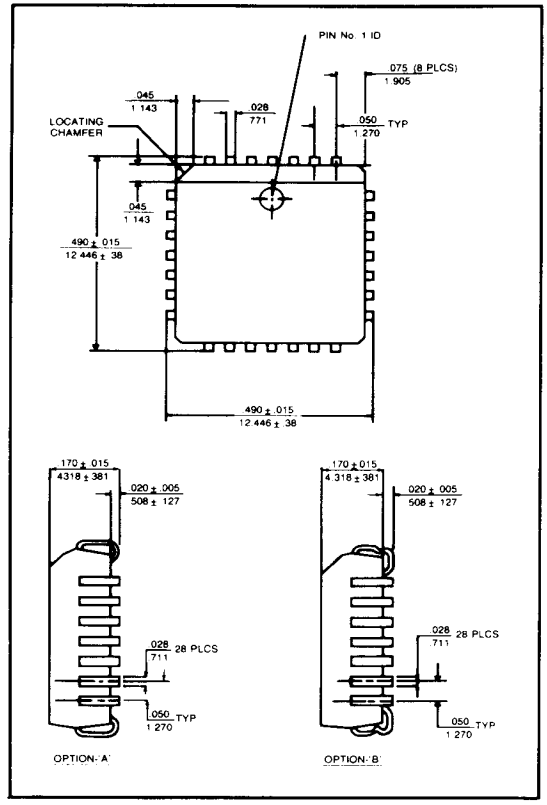
TABLE 5. DLYDR, TFULLWIN TIMING

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITION
t_{20}	DLYDR Shutoff Time	12		36	nsec	

PACKAGE DIAGRAMS



28 LEAD PLASTIC PH



28 LEAD PLASTIC QUAD JH

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